

MODEL NAME : LA-F371P non-AR  
PCB NO : DAA000EC010  
BOM P/N : 431A8C31L01

# Dell/Compal Confidential

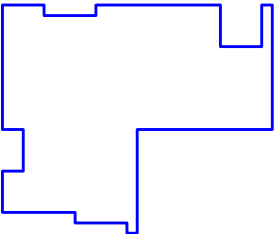
## Schematic Document

Pebble Creek MLK (Kabylake R/U)

2017-11-03

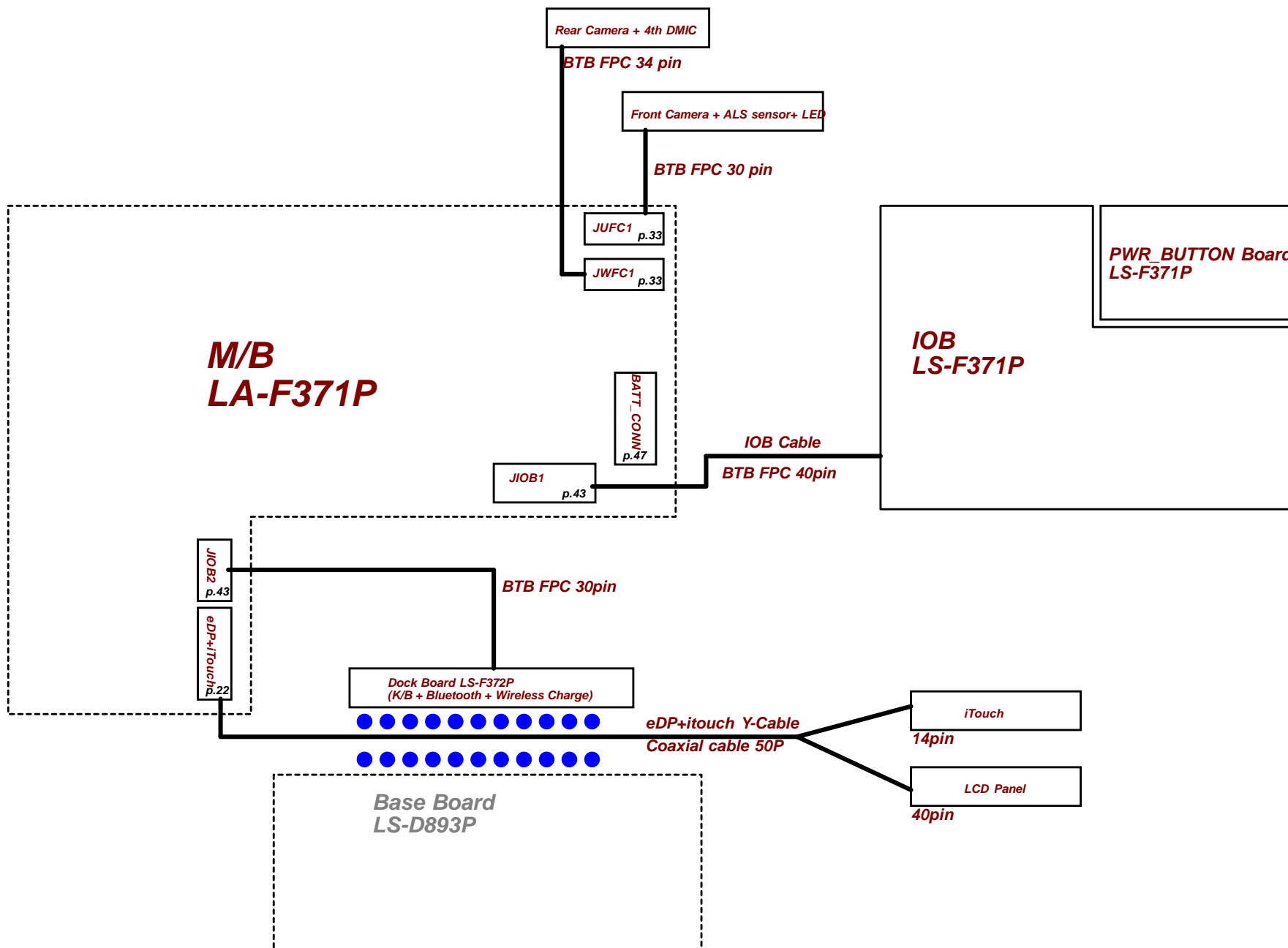
Rev: 1.0

ZZZ  
MB\_PCB



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2015/10/22	Deciphered Date	2013/10/28	Title	
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				Rev	1.0





Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	
0	240K +/- 5%	4700p		
1	130K +/- 5%	4700p	Pre-EVT1	
2	62K +/- 5%	4700p	EVT1	
3	33K +/- 5%	4700p	DVT1	
4	8.2K +/- 5%	4700p	DVT2	
5	4.3K +/- 5%	4700p	PVT	
6	2K +/- 5%	4700p		
7	NC			

Board ID Table

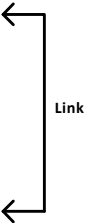
Board ID	PCB Revision
0	
1	0.1
2	0.2
3	0.3
4	0.4
5	1.0
6	
7	

USB 3.0

Flexible I/O	Interface	DESTINATION
1	USB 3.0 #1	USB Type-C Port-A
2	USB 3.0 #2/SSIC	NGFF (WWAN)
3	USB 3.0 #3	USB 3.0 Type-A
4	USB 3.0 #4	USB Type-C Port-B
5	PCI-E#1 / USB 3.0#5	Reserved for AR
6	PCI-E#2 / USB 3.0#6	Reserved for AR
7	PCI-E #3	Reserved for AR
8	PCI-E #4	Reserved for AR
9	PCI-E #5	NGFF (WLAN)
10	PCI-E #6	
11	PCI-E #7	NGFF (SSD)
12	PCI-E #8 /SATA #1	NGFF (SSD) #7/#8 2lane PCI-E
13	PCI-E #9	Card Reader
14	PCI-E #10	
15	PCI-E #11	NGFF (WWAN/2nd SSD)
16	PCI-E #12	NGFF (WWAN/2nd SSD)

SMBUS Control Table

	SOURCE	Base	BATT	Charger	XDP	USH	PD Controller	Trinity Dock	P-Sensor	MUX	IMVP	IO Expendor
No use	PCH_SML0CLK PCH_SML0DATA	PCH										
	PCH_SML1CLK PCH_SML1DATA	PCH										
	SMBCLK SMBDATA	PCH			V							
	EC_SMB00_CLK EC_SMB00_DAT	MECS105				V	V			V		
	EC_SMB01_CLK EC_SMB01_DAT	MECS105									V	
	EC_SMB02_CLK EC_SMB02_DAT	MECS105		V								V
	EC_SMB03_CLK EC_SMB03_DAT	MECS105										
	EC_SMB04_CLK EC_SMB04_DAT	MECS105					V		V	V		
	EC_SMB05_CLK EC_SMB05_DAT	MECS105	V					V				
	EC_SMB10_CLK EC_SMB10_DAT	MECS105		V								



Port Mapping USB 2.0 CLK

USB 2.0 PORT#	DESTINATION
1	Type-C Port-A
2	Dock
3	Type-C Port-B
4	WWAN
5	IR CAM
7	WLAN
9	USB Type-A
10	USH

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	
	CLKOUT_PCIE1	NGFF (WLAN)
	CLKOUT_PCIE2	NGFF (WWAN)
	CLKOUT_PCIE3	SSD
	CLKOUT_PCIE5	Card Reader
	FLEX CLOCKS	DESTINATION
	CLKOUT_LPC_0	ESPI
	CLKOUT_LPC_1	ESPI

Displayport

	DDI PORT#	DESTINATION
DDI	1	USB Type-C Port-B
	2	USB Type-C Port-A

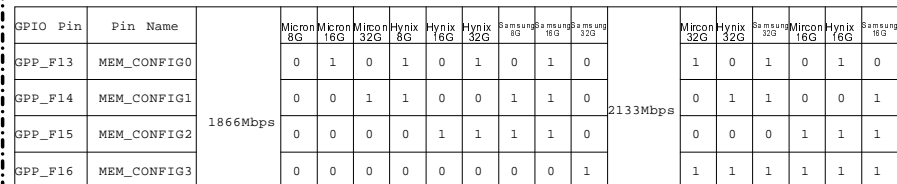
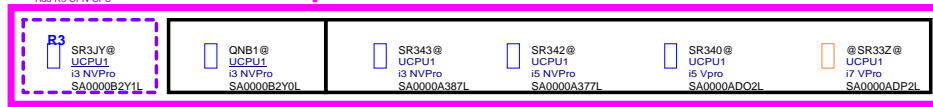
Symbol Note :

@ : means de-pop

⏏ : means Digital Ground

⏏ : means Analog Ground

### Type-C PortA



X76		DRAM Option (R1) , R3 check P08				DRAM Config Option			
						(Resistor pop location)			
		MEM_CONFIG0		MEM_CONFIG1		MEM_CONFIG2		MEM_CONFIG3	
X7669231L05	<div><div><div>MICRON_8G@U01</div><div>MT52L256M32D1PF-107WT</div><div>SA00009XUOL</div></div><div><div>MICRON_8G@U02</div><div>MT52L256M32D1PF-107WT</div><div>SA00009XUOL</div></div><div><div>MICRON_8G@U03</div><div>MT52L256M32D1PF-107WT</div><div>SA00009XUOL</div></div><div><div>MICRON_8G@U04</div><div>MT52L256M32D1PF-107WT</div><div>SA00009XUOL</div></div></div>	<div><div>X76_M8G@RH16</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_M8G@RH16</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_M8G@RH13</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_M8G@RH10</div><div>10K_0402_5%</div><div>SD028100280</div></div>							
X7669231L07	<div><div><div>MICRON_16G@U01</div><div>MT52L512M32D2PF-107WT</div><div>SA00009U7OL</div></div><div><div>MICRON_16G@U02</div><div>MT52L512M32D2PF-107WT</div><div>SA00009U7OL</div></div><div><div>MICRON_16G@U03</div><div>MT52L512M32D2PF-107WT</div><div>SA00009U7OL</div></div><div><div>MICRON_16G@U04</div><div>MT52L512M32D2PF-107WT</div><div>SA00009U7OL</div></div></div>	<div><div>X76_M16G@RH17</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_M16G@RH16</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_M16G@RH13</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_M16G@RH10</div><div>10K_0402_5%</div><div>SD028100280</div></div>							
X7669231L09	<div><div><div>MICRON_32G@U01</div><div>MT52L1G32D4PG-107WT</div><div>SA00009XYOL</div></div><div><div>MICRON_32G@U02</div><div>MT52L1G32D4PG-107WT</div><div>SA00009XYOL</div></div><div><div>MICRON_32G@U03</div><div>MT52L1G32D4PG-107WT</div><div>SA00009XYOL</div></div><div><div>MICRON_32G@U04</div><div>MT52L1G32D4PG-107WT</div><div>SA00009XYOL</div></div></div>	<div><div>X76_M32G@RH13</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_M32G@RH16</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_M32G@RH10</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_M32G@RH10</div><div>10K_0402_5%</div><div>SD028100280</div></div>							
X7669231L06	<div><div><div>HYNIX_8G@U01</div><div>H0CCNNN8GTMRLAR-NUD FBGA</div><div>SA00008G64L</div></div><div><div>HYNIX_8G@U02</div><div>H0CCNNN8GTMRLAR-NUD FBGA</div><div>SA00008G64L</div></div><div><div>HYNIX_8G@U03</div><div>H0CCNNN8GTMRLAR-NUD FBGA</div><div>SA00008G64L</div></div><div><div>HYNIX_8G@U04</div><div>H0CCNNN8GTMRLAR-NUD FBGA</div><div>SA00008G64L</div></div></div>	<div><div>X76_H8G@RH17</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_H8G@RH15</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_H8G@RH13</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_H8G@RH10</div><div>10K_0402_5%</div><div>SD028100280</div></div>							
X7669231L08	<div><div><div>HYNIX_16G@U01</div><div>H0CCNNNBUTMLAR-NUD FBGA</div><div>SA00008FJ4L</div></div><div><div>HYNIX_16G@U02</div><div>H0CCNNNBUTMLAR-NUD FBGA</div><div>SA00008FJ4L</div></div><div><div>HYNIX_16G@U03</div><div>H0CCNNNBUTMLAR-NUD FBGA</div><div>SA00008FJ4L</div></div><div><div>HYNIX_16G@U04</div><div>H0CCNNNBUTMLAR-NUD FBGA</div><div>SA00008FJ4L</div></div></div>	<div><div>X76_H16G@RH18</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_H16G@RH16</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_H16G@RH12</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_H16G@RH10</div><div>10K_0402_5%</div><div>SD028100280</div></div>							
X7669231L10	<div><div><div>HYNIX_32G@U01</div><div>H0CCNNNCLTMLAR-NUD FBGA</div><div>SA0000AENOL</div></div><div><div>HYNIX_32G@U02</div><div>H0CCNNNCLTMLAR-NUD FBGA</div><div>SA0000AENOL</div></div><div><div>HYNIX_32G@U03</div><div>H0CCNNNCLTMLAR-NUD FBGA</div><div>SA0000AENOL</div></div><div><div>HYNIX_32G@U04</div><div>H0CCNNNCLTMLAR-NUD FBGA</div><div>SA0000AENOL</div></div></div>	<div><div>X76_H32G@RH17</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_H32G@RH16</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_H32G@RH13</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_H32G@RH10</div><div>10K_0402_5%</div><div>SD028100280</div></div>							
X7669231L01	<div><div><div>X76_8G@X76G</div><div>X76</div><div>X7669231L01</div></div><div><div>SAMSUNG_8G@U01</div><div>K4E8E304EB-EGCF FBGA178</div><div>SA00009XYOL</div></div><div><div>SAMSUNG_8G@U02</div><div>K4E8E304EB-EGCF FBGA178</div><div>SA00009XYOL</div></div><div><div>SAMSUNG_8G@U03</div><div>K4E8E304EB-EGCF FBGA178</div><div>SA00009XYOL</div></div><div><div>SAMSUNG_8G@U04</div><div>K4E8E304EB-EGCF FBGA178</div><div>SA00009XYOL</div></div></div>	<div><div>X76_S8G@RH18</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_S8G@RH15</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_S8G@RH12</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_S8G@RH10</div><div>10K_0402_5%</div><div>SD028100280</div></div>							
X7669231L02	<div><div><div>X76_16G@X7616G</div><div>X76</div><div>X7669231L02</div></div><div><div>SAMSUNG_16G@U01</div><div>K4E6B304EB-EGCF FBGA17</div><div>SA00008QV2L</div></div><div><div>SAMSUNG_16G@U02</div><div>K4E6B304EB-EGCF FBGA17</div><div>SA00008QV2L</div></div><div><div>SAMSUNG_16G@U03</div><div>K4E6B304EB-EGCF FBGA17</div><div>SA00008QV2L</div></div><div><div>SAMSUNG_16G@U04</div><div>K4E6B304EB-EGCF FBGA17</div><div>SA00008QV2L</div></div></div>	<div><div>X76_S16G@RH17</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_S16G@RH16</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_S16G@RH13</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_S16G@RH10</div><div>10K_0402_5%</div><div>SD028100280</div></div>							
X7669231L03	<div><div><div>X76_32G@X7632G</div><div>X76</div><div>X7669231L03</div></div><div><div>SAMSUNG_32G@U01</div><div>4EBE304EB-EGCF FBGA178</div><div>SA00008X1OL</div></div><div><div>SAMSUNG_32G@U02</div><div>4EBE304EB-EGCF FBGA178</div><div>SA00008X1OL</div></div><div><div>SAMSUNG_32G@U03</div><div>4EBE304EB-EGCF FBGA178</div><div>SA00008X1OL</div></div><div><div>SAMSUNG_32G@U04</div><div>4EBE304EB-EGCF FBGA178</div><div>SA00008X1OL</div></div></div>	<div><div>X76_S32G@RH18</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_S32G@RH16</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_S32G@RH13</div><div>10K_0402_5%</div><div>SD028100280</div></div> <div><div>X76_S32G@RH9</div><div>10K_0402_5%</div><div>SD028100280</div></div>							

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Issued Date	2015/10/22	Deciphered Date	2013/10/28	Title	P05-MCP(1/14)DDI,EDP,CS12,EMMC	
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# LPDDR3, Ballout for side by side(Non-Interleave)

19	DDR_A_DQS#0..7	19	DDR_B_DQS#0..7
19	DDR_A_DQS#0..7	20	DDR_B_DQS#0..7
19	DDR_A_DQ0..63	20	DDR_B_DQ0..63
19,21	DDR_A_CA1_0..9	20,21	DDR_B_CA1_0..9
19,21	DDR_A_CA2_0..9	20,21	DDR_B_CA2_0..9

@UCPU1B

SKL-U

DDR_A_D0	AL71	DDR0_CK0[0]	AU53	DDR_A_CLK#0	19,21
DDR_A_D1	AL68	DDR0_CK0[1]	AT53	DDR_A_CLK#1	19,21
DDR_A_D2	AN68	DDR0_CK0[2]	AU55	DDR_A_CLK#2	19,21
DDR_A_D3	AN69	DDR0_CK0[3]	AT55	DDR_A_CLK#3	19,21
DDR_A_D4	AL70	DDR0_CK0[4]	BA56	DDR_A_CKE0	19,21
DDR_A_D5	AL69	DDR0_CK0[5]	B856	DDR_A_CKE1	19,21
DDR_A_D6	AN70	DDR0_CK0[6]	AW56	DDR_A_CKE2	19,21
DDR_A_D7	AN71	DDR0_CK0[7]	AY56	DDR_A_CKE3	19,21
DDR_A_D8	AR70	DDR0_CK0[8]	AU46	DDR_A_CS#0	19,21
DDR_A_D9	AR68	DDR0_CK0[9]	AU43	DDR_A_CS#1	19,21
DDR_A_D10	AU71	DDR0_CK0[10]	AT45	DDR_A_CS#1	19,21
DDR_A_D11	AU68	DDR0_CK0[11]	AT43	DDR_A_ODT0	19,21
DDR_A_D12	AR71	DDR0_CK0[12]	BA51		
DDR_A_D13	AR69	DDR0_CK0[13]	B851		
DDR_A_D14	AU70	DDR0_CK0[14]	BA52		
DDR_A_D15	AU69	DDR0_CK0[15]	AY52		
DDR_A_D16	AW65	DDR0_CK0[16]	AW52		
DDR_A_D17	AW63	DDR0_CK0[17]	AW52		
DDR_A_D18	AY63	DDR0_CK0[18]	AW52		
DDR_A_D19	BA65	DDR0_CK0[19]	AW54		
DDR_A_D20	AY65	DDR0_CK0[20]	BA54		
DDR_A_D21	BA63	DDR0_CK0[21]	BA55		
DDR_A_D22	BB63	DDR0_CK0[22]	AY54		
DDR_A_D23	BA61	DDR0_CK0[23]	AU46		
DDR_A_D24	AW61	DDR0_CK0[24]	AU46		
DDR_A_D25	BB69	DDR0_CK0[25]	AU48		
DDR_A_D26	AW59	DDR0_CK0[26]	AT48		
DDR_A_D27	BB61	DDR0_CK0[27]	AY59		
DDR_A_D28	AY61	DDR0_CK0[28]	BB50		
DDR_A_D29	BA59	DDR0_CK0[29]	BA50		
DDR_A_D30	AY59	DDR0_CK0[30]	BB52		
DDR_B_D0	AY39	DDR0_CK0[31]	AM70		
DDR_B_D1	AW39	DDR0_CK0[32]	AM69		
DDR_B_D2	AY37	DDR0_CK0[33]	AT69		
DDR_B_D3	AY37	DDR0_CK0[34]	AT70		
DDR_B_D4	BB39	DDR0_CK0[35]	BA64		
DDR_B_D5	BA39	DDR0_CK0[36]	AY64		
DDR_B_D6	BA37	DDR0_CK0[37]	AY60		
DDR_B_D7	BB37	DDR0_CK0[38]	BA60		
DDR_B_D8	AY35	DDR0_CK0[39]	BA38		
DDR_B_D9	AW35	DDR0_CK0[40]	AY38		
DDR_B_D10	AY33	DDR0_CK0[41]	AY34		
DDR_B_D11	AW33	DDR0_CK0[42]	BA34		
DDR_B_D12	BB35	DDR0_CK0[43]	BA30		
DDR_B_D13	BA35	DDR0_CK0[44]	AY30		
DDR_B_D14	BA33	DDR0_CK0[45]	AY26		
DDR_B_D15	BB33	DDR0_CK0[46]	BA26		
DDR_B_D16	AY31	DDR0_CK0[47]	AW50		
DDR_B_D17	AW31	DDR0_CK0[48]	AT52		
DDR_B_D18	AY29	DDR0_CK0[49]	AY67		
DDR_B_D19	AW29	DDR0_CK0[50]	AY68		
DDR_B_D20	BB29	DDR0_CK0[51]	BA67		
DDR_B_D21	BA29	DDR0_CK0[52]			
DDR_B_D22	BB27	DDR0_CK0[53]			
DDR_B_D23	BA27	DDR0_CK0[54]			
DDR_B_D24	BB25	DDR0_CK0[55]			
DDR_B_D25		DDR0_CK0[56]			

SKL-U\_BGA1356

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@UCPU1C

SKL-U

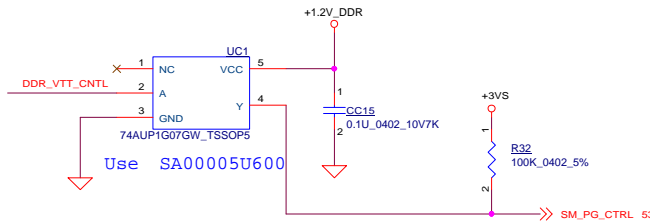
DDR_A_D16	AF65	DDR1_CK0[0]	AN46	DDR_B_CLK#0	20,21
DDR_A_D17	AF64	DDR1_CK0[1]	AN46	DDR_B_CLK#1	20,21
DDR_A_D18	AK65	DDR1_CK0[2]	AP45	DDR_B_CLK#2	20,21
DDR_A_D19	AK64	DDR1_CK0[3]	AP46	DDR_B_CLK#3	20,21
DDR_A_D20	AF66	DDR1_CK0[4]	AP46	DDR_B_CLK#4	20,21
DDR_A_D21	AF67	DDR1_CK0[5]	AN56	DDR_B_CKE0	20,21
DDR_A_D22	AK67	DDR1_CK0[6]	AP56	DDR_B_CKE1	20,21
DDR_A_D23	AK66	DDR1_CK0[7]	AN55	DDR_B_CKE2	20,21
DDR_A_D24	AF70	DDR1_CK0[8]	AP53	DDR_B_CKE3	20,21
DDR_A_D25	AF68	DDR1_CK0[9]	BB42	DDR_B_CS#0	20,21
DDR_A_D26	AH71	DDR1_CK0[10]	AY42	DDR_B_CS#1	20,21
DDR_A_D27	AH68	DDR1_CK0[11]	BA42	DDR_B_ODT0	20,21
DDR_A_D28	AF69	DDR1_CK0[12]	AW42		
DDR_A_D29	AH70	DDR1_CK0[13]	AY48		
DDR_A_D30	AH70	DDR1_CK0[14]	AP50		
DDR_A_D31	AH69	DDR1_CK0[15]	BA48		
DDR_A_D32	AU66	DDR1_CK0[16]	BB48		
DDR_A_D33	AP65	DDR1_CK0[17]	AP48		
DDR_A_D34	AN65	DDR1_CK0[18]	AN50		
DDR_A_D35	AN66	DDR1_CK0[19]	AN48		
DDR_A_D36	AT65	DDR1_CK0[20]	AN53		
DDR_A_D37	AU65	DDR1_CK0[21]	AN52		
DDR_A_D38	AT61	DDR1_CK0[22]	BA43		
DDR_A_D39	AN60	DDR1_CK0[23]	AY43		
DDR_A_D40	AN61	DDR1_CK0[24]	AY44		
DDR_A_D41	AT60	DDR1_CK0[25]	AW44		
DDR_A_D42	AT60	DDR1_CK0[26]	BB44		
DDR_A_D43	AU60	DDR1_CK0[27]	AY47		
DDR_A_D44	AU60	DDR1_CK0[28]	BA44		
DDR_A_D45	AT40	DDR1_CK0[29]	AW46		
DDR_A_D46	AT40	DDR1_CK0[30]	AY46		
DDR_A_D47	AT40	DDR1_CK0[31]	BA46		
DDR_A_D48	AT40	DDR1_CK0[32]	BB46		
DDR_A_D49	AT40	DDR1_CK0[33]	BA47		
DDR_A_D50	AT40	DDR1_CK0[34]	AH66		
DDR_A_D51	AT40	DDR1_CK0[35]	AH65		
DDR_A_D52	AT40	DDR1_CK0[36]	AG69		
DDR_A_D53	AT40	DDR1_CK0[37]	AG70		
DDR_A_D54	AT40	DDR1_CK0[38]	AR63		
DDR_A_D55	AT40	DDR1_CK0[39]	AR65		
DDR_A_D56	AT40	DDR1_CK0[40]	AR61		
DDR_A_D57	AT40	DDR1_CK0[41]	AR60		
DDR_A_D58	AT40	DDR1_CK0[42]	AT39		
DDR_A_D59	AT40	DDR1_CK0[43]	AR38		
DDR_A_D60	AT40	DDR1_CK0[44]	AT32		
DDR_A_D61	AT40	DDR1_CK0[45]	AR26		
DDR_A_D62	AT40	DDR1_CK0[46]	AR27		
DDR_A_D63	AT40	DDR1_CK0[47]	AR22		
DDR_A_D64	AT40	DDR1_CK0[48]	AR21		
DDR_A_D65	AT40	DDR1_CK0[49]	AN43		
DDR_A_D66	AT40	DDR1_CK0[50]	AP43		
DDR_A_D67	AT40	DDR1_CK0[51]	AT13		
DDR_A_D68	AT40	DDR1_CK0[52]	DRAM_RESET#		
DDR_A_D69	AT40	DDR1_CK0[53]	DDR_RCOMP[0]		
DDR_A_D70	AT40	DDR1_CK0[54]	DDR_RCOMP[1]		
DDR_A_D71	AT40	DDR1_CK0[55]	DDR_RCOMP[2]		
DDR_A_D72	AT40	DDR1_CK0[56]			
DDR_A_D73	AT40	DDR1_CK0[57]			
DDR_A_D74	AT40	DDR1_CK0[58]			
DDR_A_D75	AT40	DDR1_CK0[59]			
DDR_A_D76	AT40	DDR1_CK0[60]			
DDR_A_D77	AT40	DDR1_CK0[61]			
DDR_A_D78	AT40	DDR1_CK0[62]			
DDR_A_D79	AT40	DDR1_CK0[63]			

SKL-U\_BGA1356

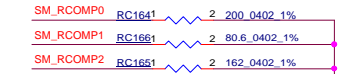
3 OF 20

DDR CH - A

DDR CH - B



## LPDDR3 COMPENSATION SIGNALS



CAD Note:  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

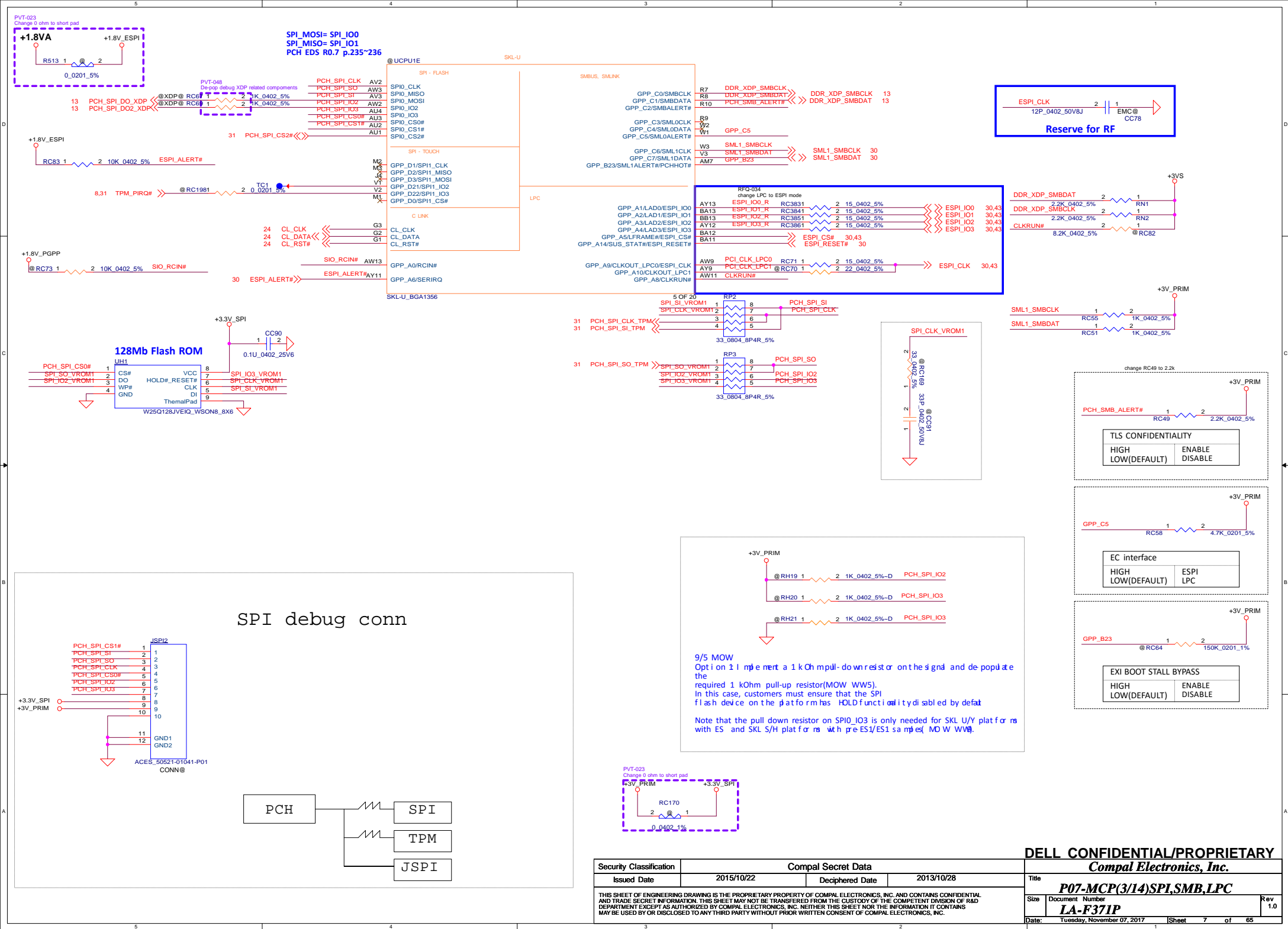
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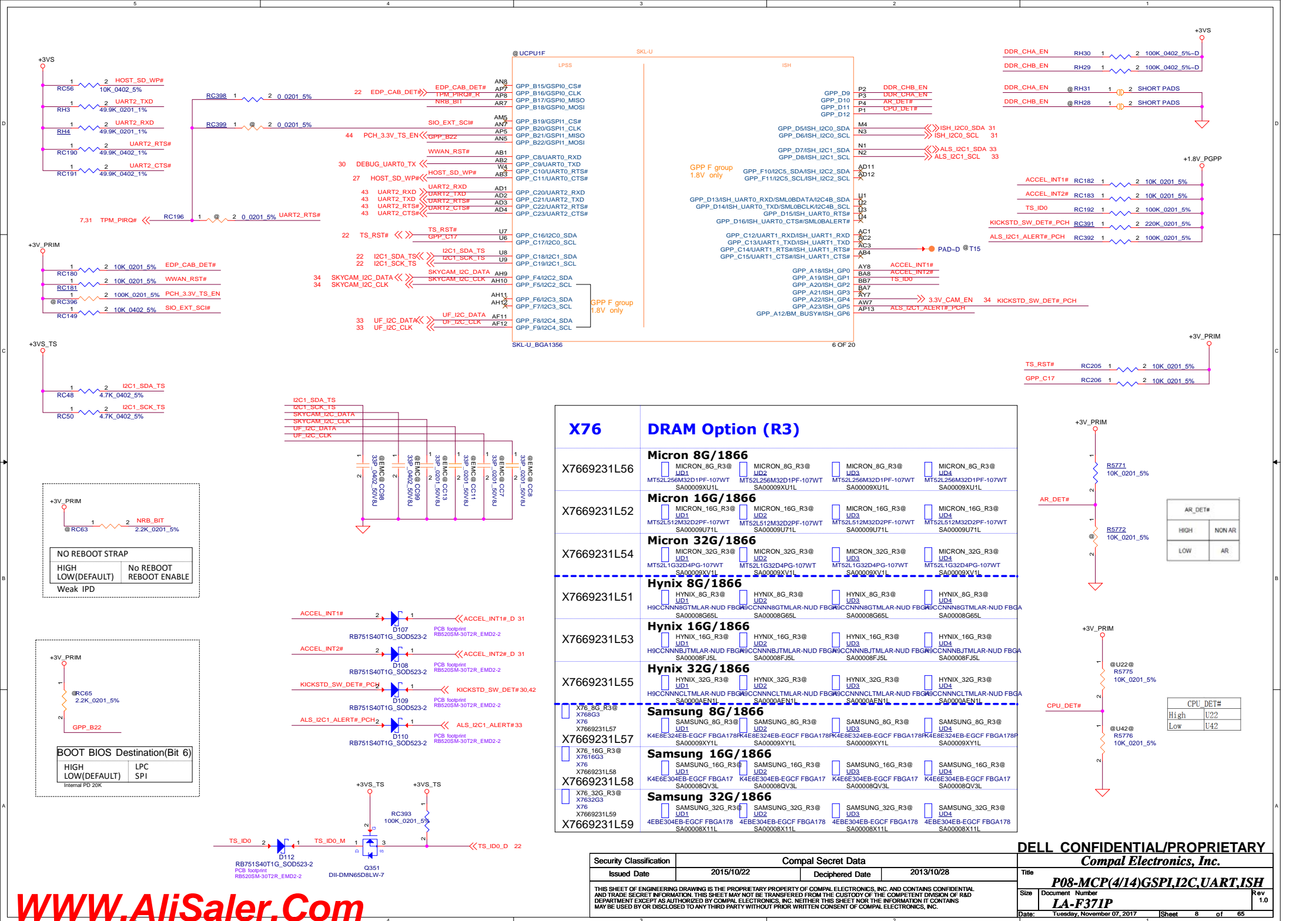
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Issued Date	2015/10/22	Deciphered Date
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M.2 2242  
WWAN 2nd  
SSD SATA/PCIe 2 Lane only 4/14

PCIe SSD

SATA SSD  
Cardreader  
PCIe Gen2 x 1

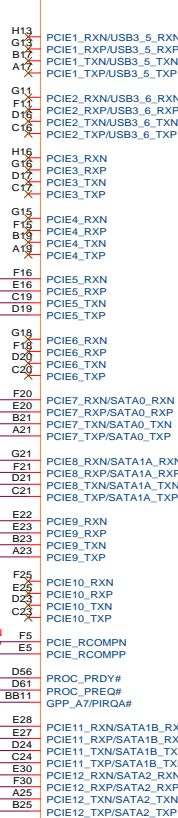
WLAN  
PCIe Gen2 x 1

@UCPU1H

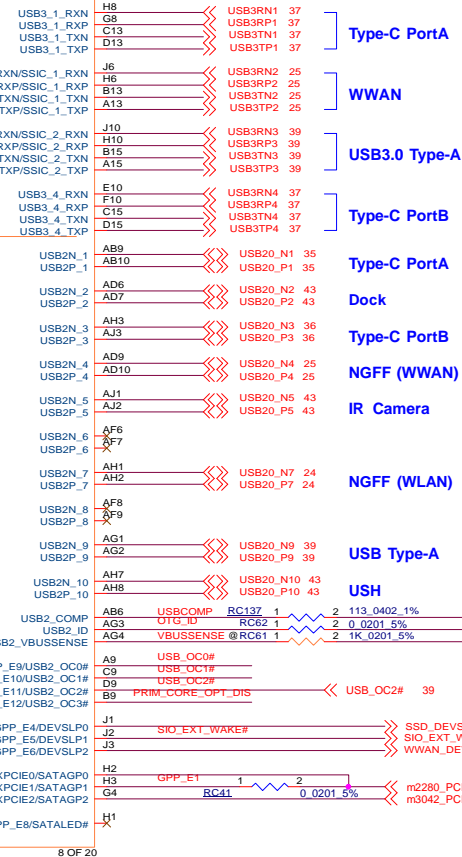
SKL-U

PCIe/USB3/SATA

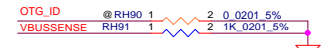
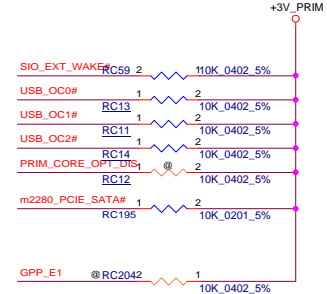
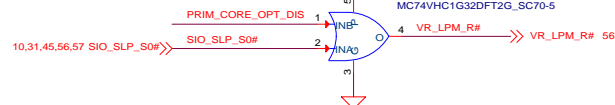
SSIC / USB3



USB2



10,31,45,56,57 SIO\_SLP\_S0#

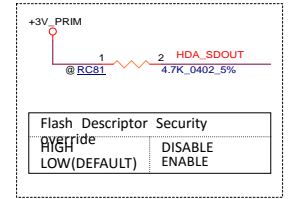
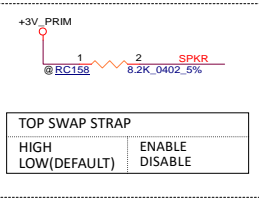
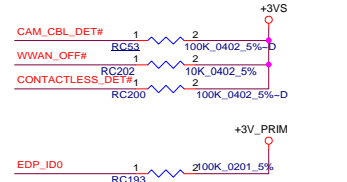
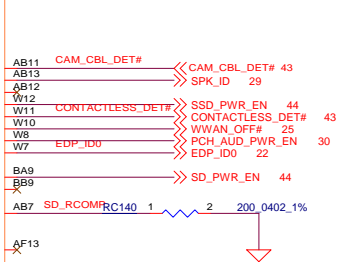
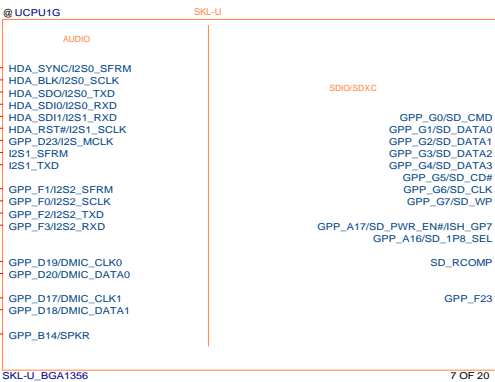
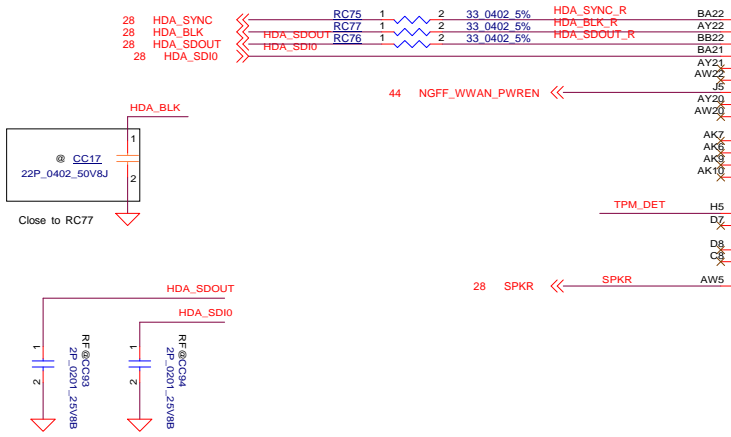
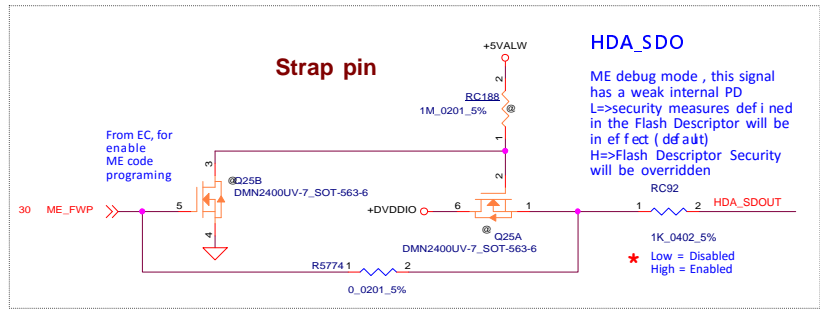
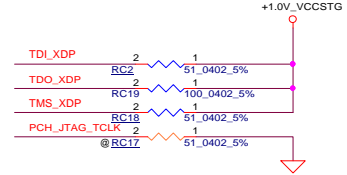
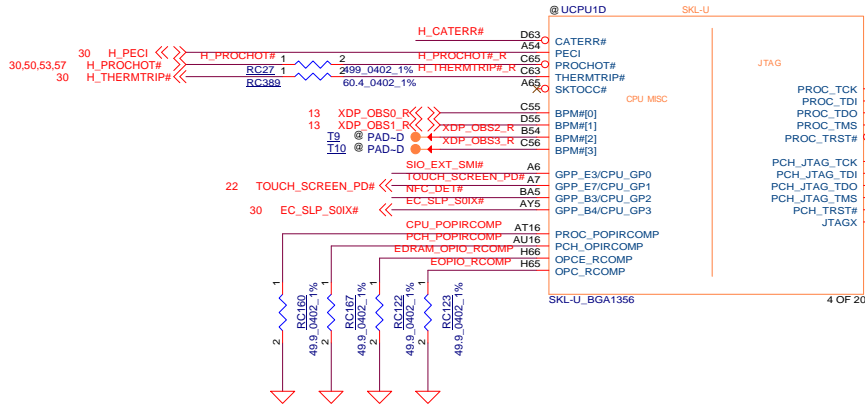
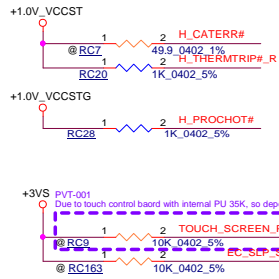


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Size	Document	Number
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### TPM BOM Optional

TPM_DET	
TPM	1 = W/TPM 0 = W/O TPM

TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Flash Descriptor Security	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

Security Classification		Compal Secret Data	
Issued Date	2015/10/22	Deciphered Date	2013/10/28
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Title	P11-MCP(7/14)MISC,JTAG,HDA,SDIO		
Size	Document Number	Rev	
	LA-F371P	1.0	
Date:	Tuesday, November 07, 2017	Sheet	11 of 65



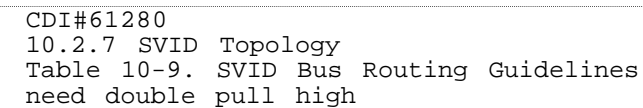


**Component placement order:**  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

The diagram illustrates the CPU power plane for a SKYLAKE-U 2+3e processor. It shows the power distribution from the +VCC\_CORE and +VCC\_CORE\_G0/G1 inputs through various decoupling capacitors and sense resistors to the CPU power pins. Key components include 100nF capacitors for VCC, 100uF capacitors for VSS, and 0.0402 1% resistors for current sensing. The diagram is labeled with SKL-U, SKL-U\_BGA1356, and 12 OF 20.

**Power Plane Components:**

- Inputs:** +VCC\_CORE, +VCC\_CORE\_G0, +VCC\_CORE\_G1, +1.0V\_VCCSTG\_R, +1.0V\_VCCSTG.
- Capacitors:** 100nF (VCC), 100uF (VSS), 0.0402 1% (resistors).
- Resistors:** 100uF (VSS), 0.0402 1% (resistors).
- Labels:** SKL-U, SKL-U\_BGA1356, 12 OF 20.

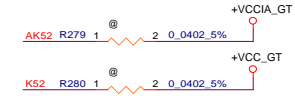
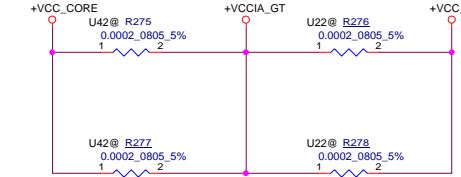
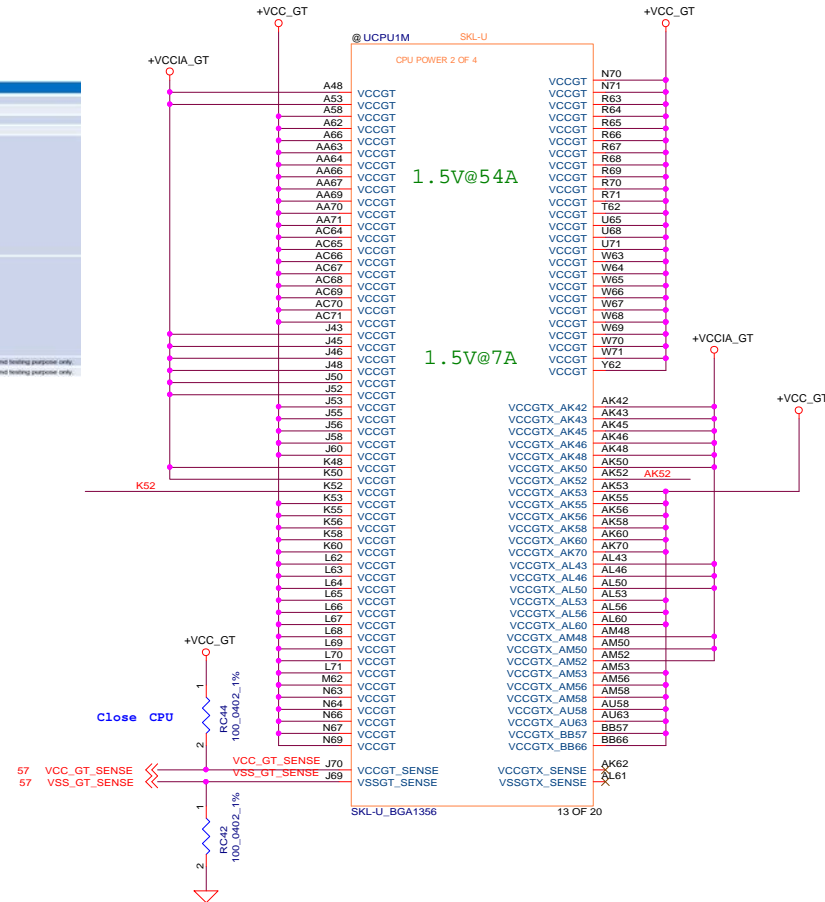


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				<b>LA-F371P</b>	
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+VCCGT: 0.55~1.5V, 54A  
+VCCGTx : 0.55~1.5V, 7A

Ball #	Ball Names R-J447	Ball Names U22	R-J443/U22 common board guidelines
C7	XTAL24_OUT	NC	connected to R-J443 XTAL24_OUT
C8	XTAL24_IN	NC	connected to R-J443 XTAL24_IN
C18	NC	XTAL24_OUT	connected to U22 XTAL24_OUT
C17	NC	XTAL24_IN	connected to U22 XTAL24_IN
A443	VCC000RE	VSS00Tx	
AA43	VCC000RE	VSS0Tx	
AA42	VCC000RE	VSS0Tx	
AA41	VCC000RE	VSS0Tx	
AA40	VCC000RE	VSS0Tx	
AA39	VCC000RE	VSS0Tx	
AA38	VCC000RE	VSS0Tx	
AA37	VCC000RE	VSS0Tx	
AA36	VCC000RE	VSS0Tx	
AA35	VCC000RE	VSS0Tx	
AA34	VCC000RE	VSS0Tx	
AA33	VCC000RE	VSS0Tx	
AA32	VCC000RE	VSS0Tx	
AA31	VCC000RE	VSS0Tx	
AA30	VCC000RE	VSS0Tx	
AA29	VCC000RE	VSS0Tx	
AA28	VCC000RE	VSS0Tx	
AA27	VCC000RE	VSS0Tx	
AA26	VCC000RE	VSS0Tx	
AA25	VCC000RE	VSS0Tx	
AA24	VCC000RE	VSS0Tx	
AA23	VCC000RE	VSS0Tx	
AA22	VCC000RE	VSS0Tx	
AA21	VCC000RE	VSS0Tx	
AA20	VCC000RE	VSS0Tx	
AA19	VCC000RE	VSS0Tx	
AA18	VCC000RE	VSS0Tx	
AA17	VCC000RE	VSS0Tx	
AA16	VCC000RE	VSS0Tx	
AA15	VCC000RE	VSS0Tx	
AA14	VCC000RE	VSS0Tx	
AA13	VCC000RE	VSS0Tx	
AA12	VCC000RE	VSS0Tx	
AA11	VCC000RE	VSS0Tx	
AA10	VCC000RE	VSS0Tx	
AA9	VCC000RE	VSS0Tx	
AA8	VCC000RE	VSS0Tx	
AA7	VCC000RE	VSS0Tx	
AA6	VCC000RE	VSS0Tx	
AA5	VCC000RE	VSS0Tx	
AA4	VCC000RE	VSS0Tx	
AA3	VCC000RE	VSS0Tx	
AA2	VCC000RE	VSS0Tx	
AA1	VCC000RE	VSS0Tx	
AA0	VCC000RE	VSS0Tx	
AA-1	VCC000RE	VSS0Tx	
AA-2	VCC000RE	VSS0Tx	
AA-3	VCC000RE	VSS0Tx	
AA-4	VCC000RE	VSS0Tx	
AA-5	VCC000RE	VSS0Tx	
AA-6	VCC000RE	VSS0Tx	
AA-7	VCC000RE	VSS0Tx	
AA-8	VCC000RE	VSS0Tx	
AA-9	VCC000RE	VSS0Tx	
AA-10	VCC000RE	VSS0Tx	
AA-11	VCC000RE	VSS0Tx	
AA-12	VCC000RE	VSS0Tx	
AA-13	VCC000RE	VSS0Tx	
AA-14	VCC000RE	VSS0Tx	
AA-15	VCC000RE	VSS0Tx	
AA-16	VCC000RE	VSS0Tx	
AA-17	VCC000RE	VSS0Tx	
AA-18	VCC000RE	VSS0Tx	
AA-19	VCC000RE	VSS0Tx	
AA-20	VCC000RE	VSS0Tx	
AA-21	VCC000RE	VSS0Tx	
AA-22	VCC000RE	VSS0Tx	
AA-23	VCC000RE	VSS0Tx	
AA-24	VCC000RE	VSS0Tx	
AA-25	VCC000RE	VSS0Tx	
AA-26	VCC000RE	VSS0Tx	
AA-27	VCC000RE	VSS0Tx	
AA-28	VCC000RE	VSS0Tx	
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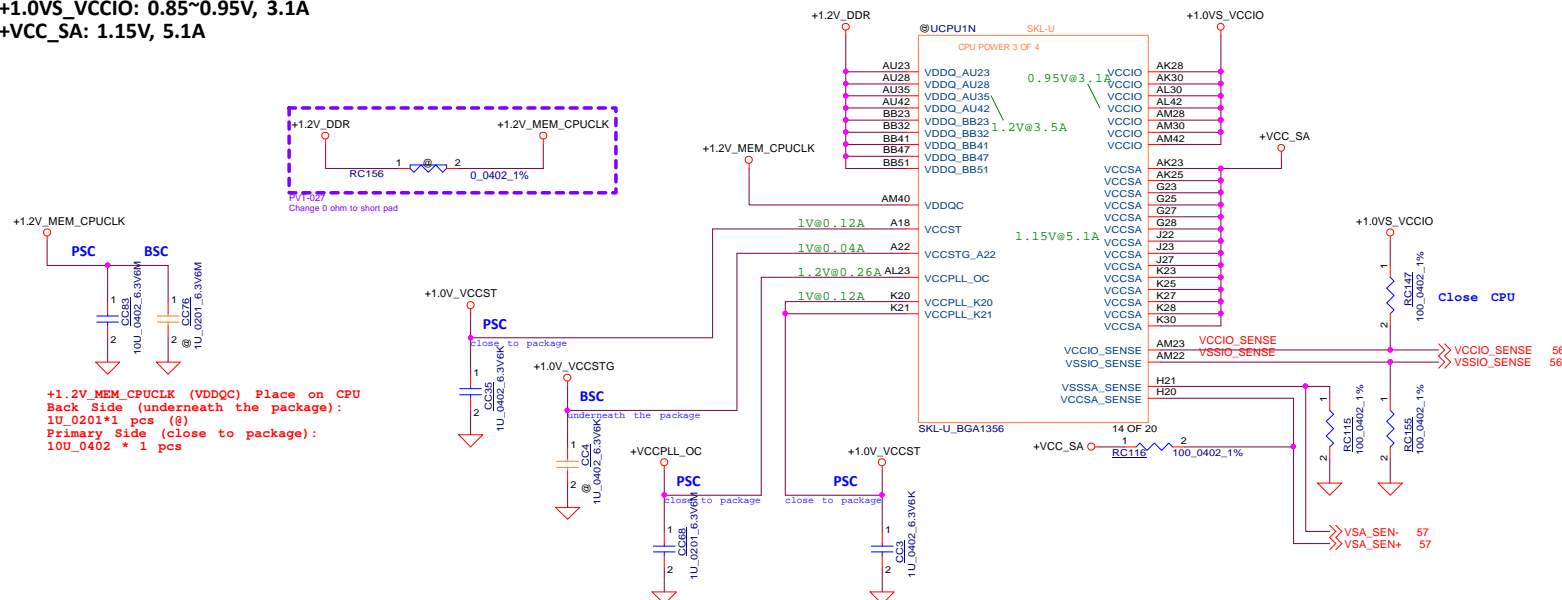


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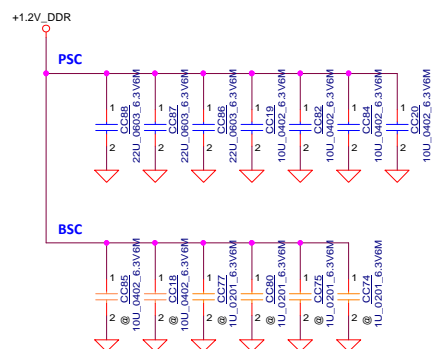
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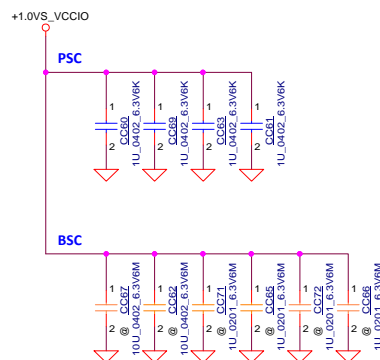
+1.2V\_DDR: 1.2V, 3.5A  
 +1.0V\_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA  
 +1.0V\_VCCSTG: 1V, 40mA  
 +VCCPLL\_OC: 1.2V, 260mA  
 +1.0VS\_VCCIO: 0.85~0.95V, 3.1A  
 +VCC\_SA: 1.15V, 5.1A



+1.2V\_DDR Decoupling Requirement  
 Back Side (underneath the package):  
 10U\_0402\*2 pcs + 1U\_0201\*4 pcs (8)  
 Primary Side (close to package):  
 10U\_0402\*4 pcs + 22U\_0603\*3 pcs



+1.0VS\_VCCIO Decoupling Requirement  
 Back Side (underneath the package):  
 10U\_0402\*2 pcs + 1U\_0201\*4 pcs (8)  
 Primary Side (close to package):  
 1U\_0402\*4 pcs



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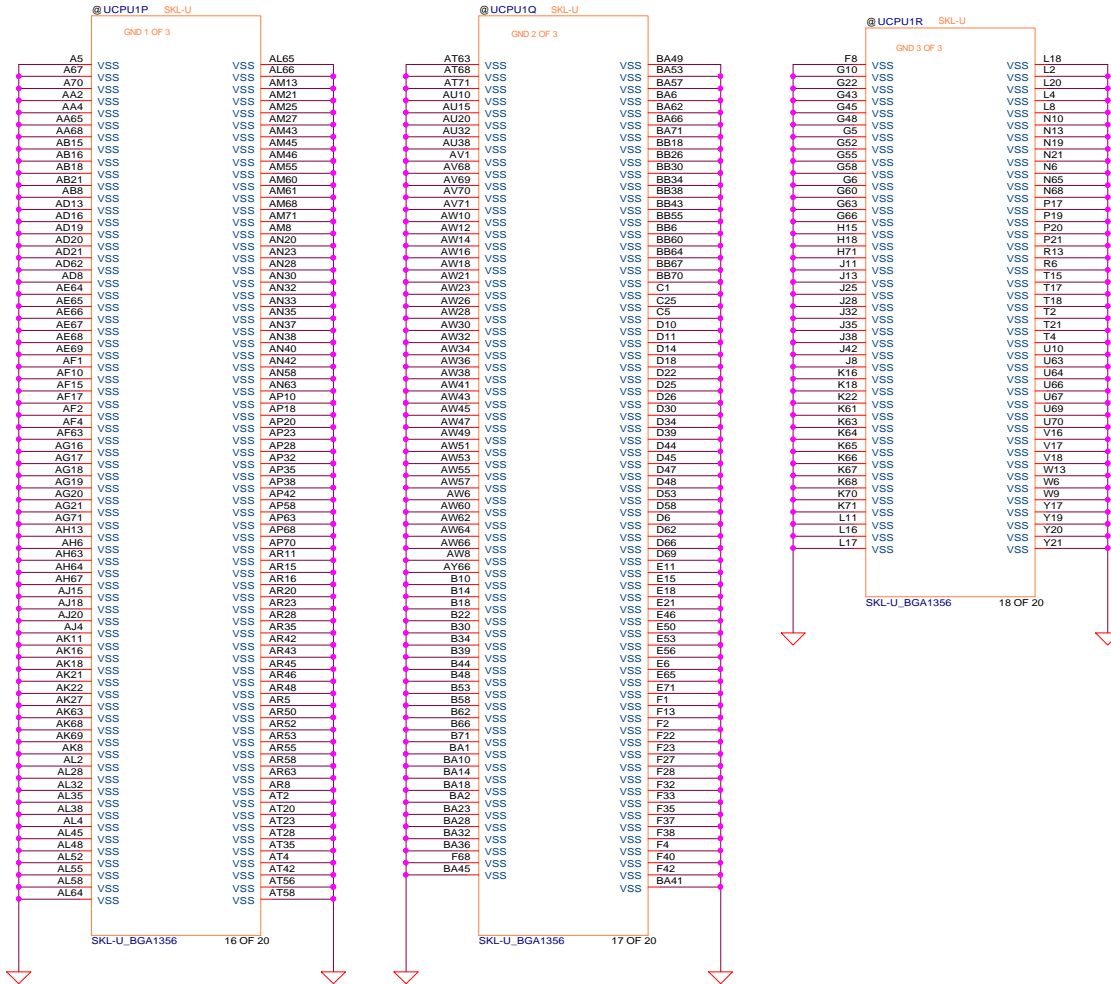
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Title	P16-MCP(12/14)PWR-VCCIO.MEM		
Size	Document Number	Rev	1.0
Date:	Tuesday, November 07, 2017	Sheet	16 of 65



Note1: VCCPRIM\_CORE Implementat i on út h PCH CORE\_V D Reco mnendat i on

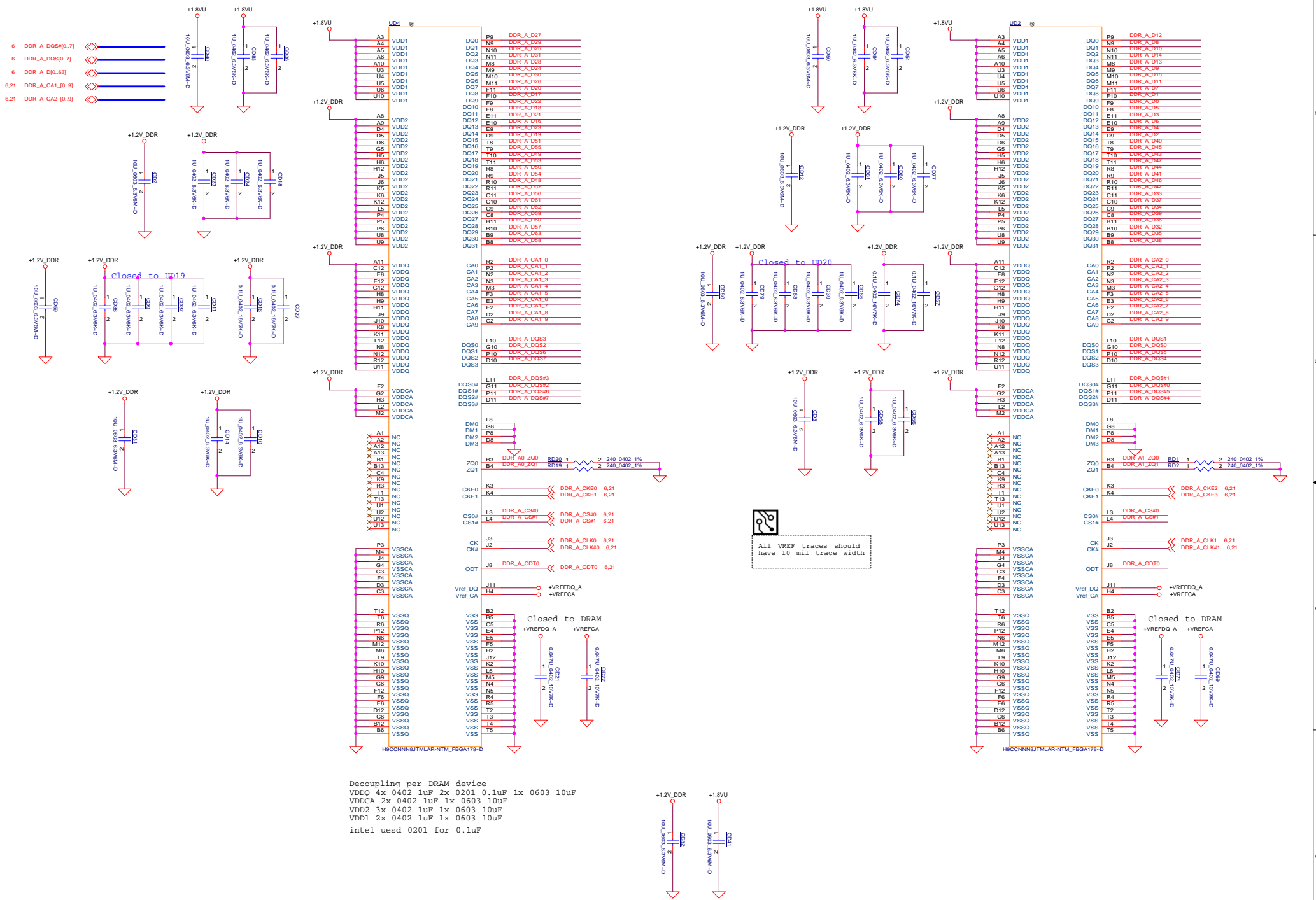
R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



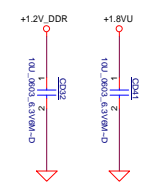
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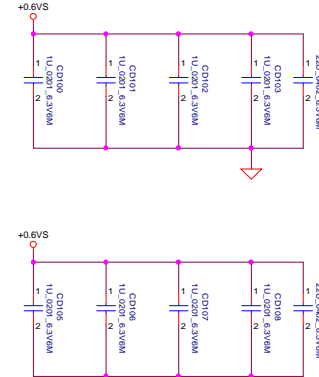
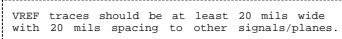


Decoupling per DRAM device  
VDDQ 4x 0402 1uF 2x 0201 0.1uF 1x 0603 10uF  
VDDCA 2x 0402 1uF 1x 0603 10uF  
VDD2 3x 0402 1uF 1x 0603 10uF  
VDD1 2x 0402 1uF 1x 0603 10uF  
intel used 0201 for 0.1uF



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Issued Date	2015/10/22	Deciphered Date	2013/10/28
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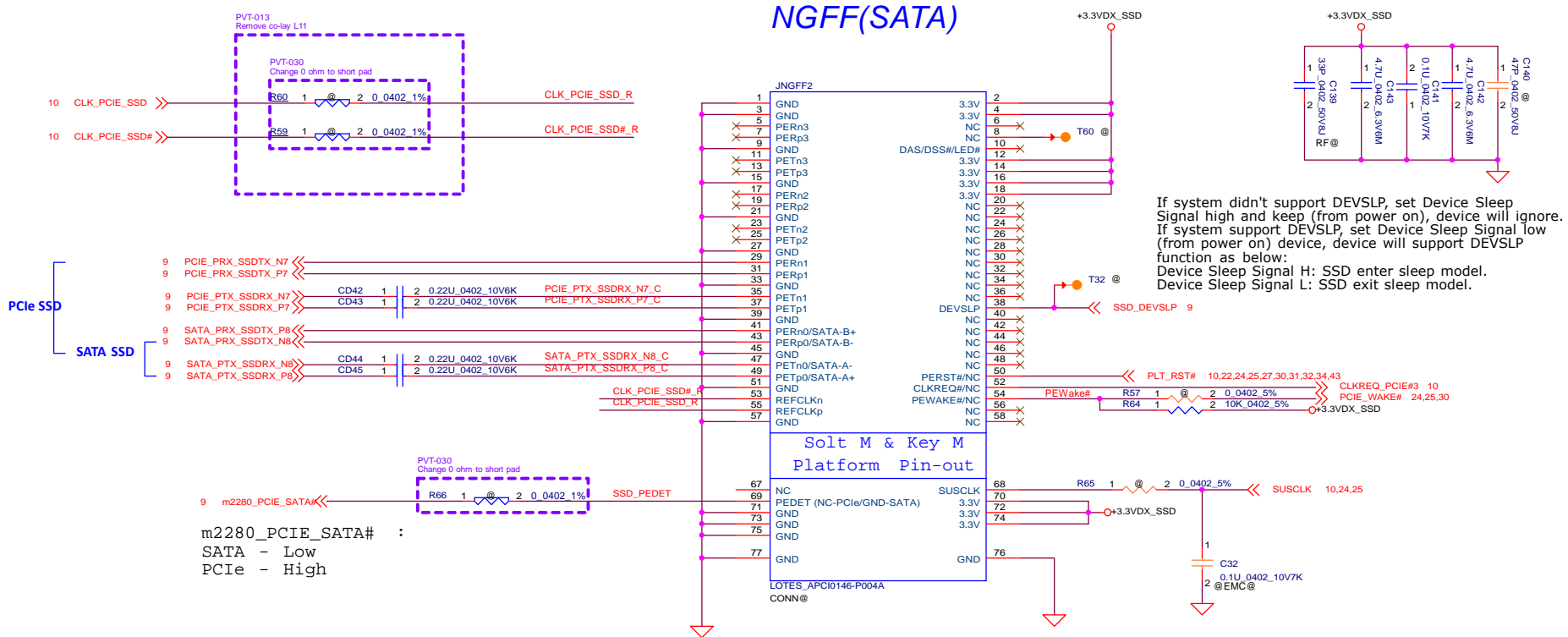


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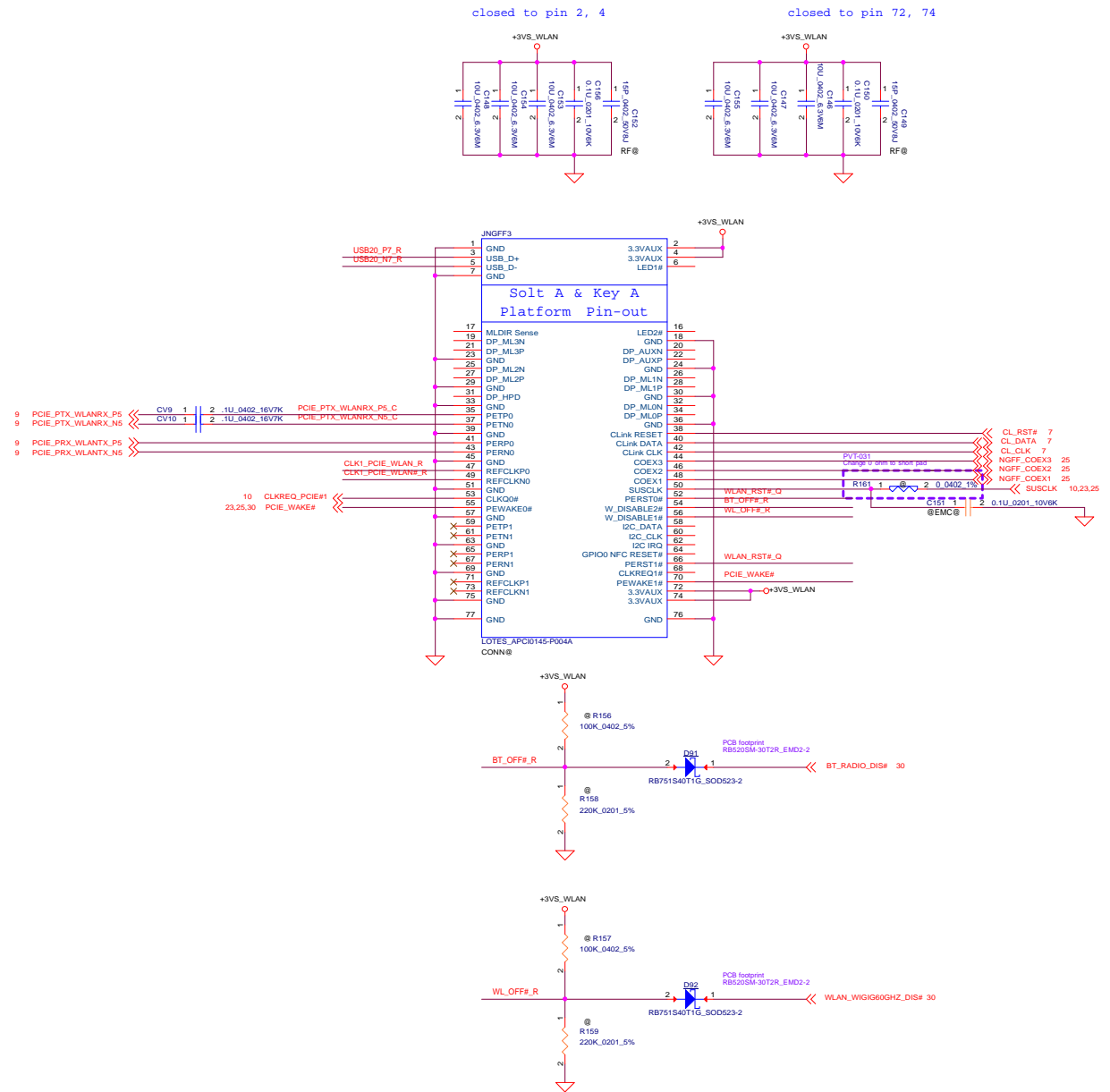
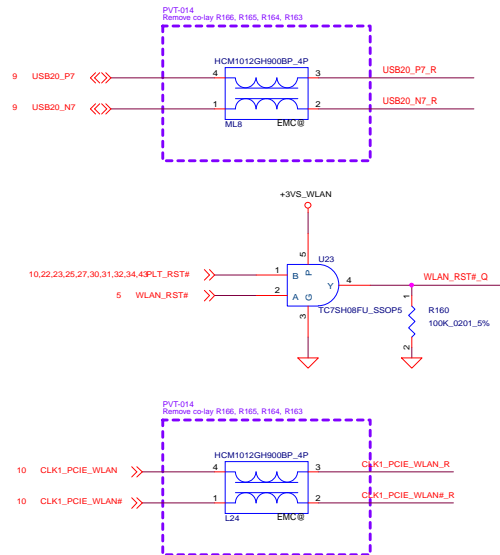
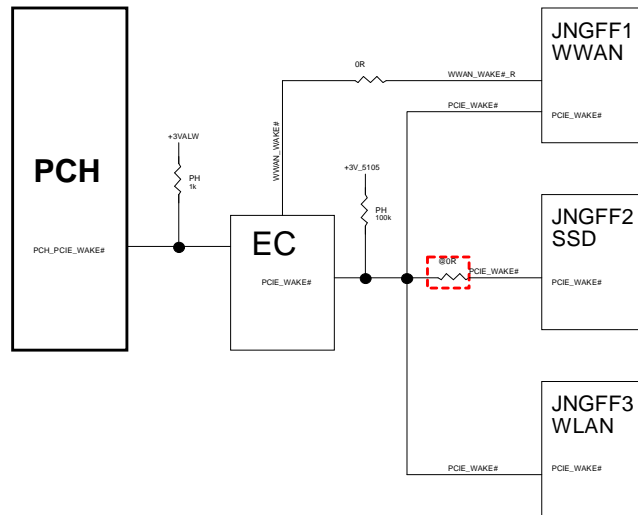


TVN1S2302ABQ SOT523-3

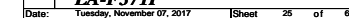




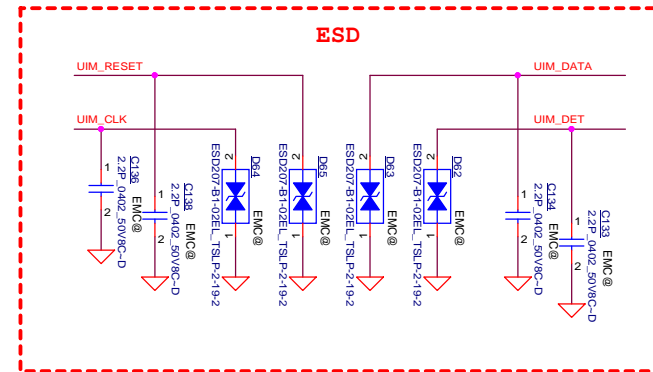
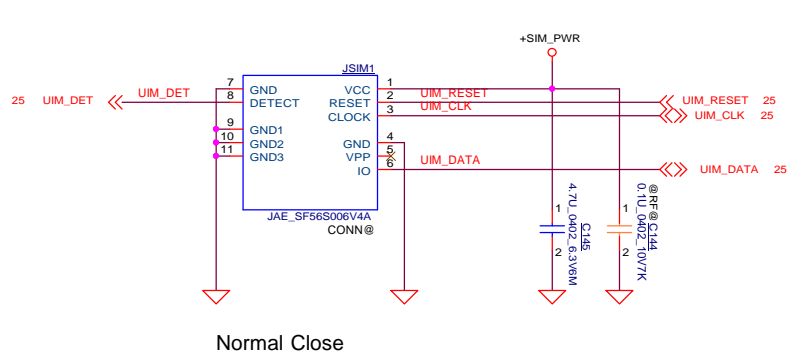
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Issued Date		2015/10/22		Deciphered Date		2013/10/28		Title		P23-SATA / PCIE SSD			
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				Size Document Number
				LA-F371P
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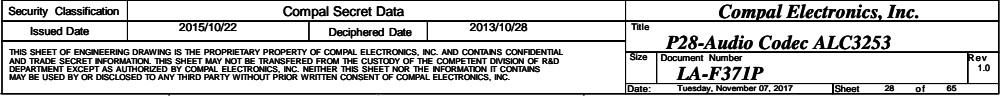


# uSIM CONN



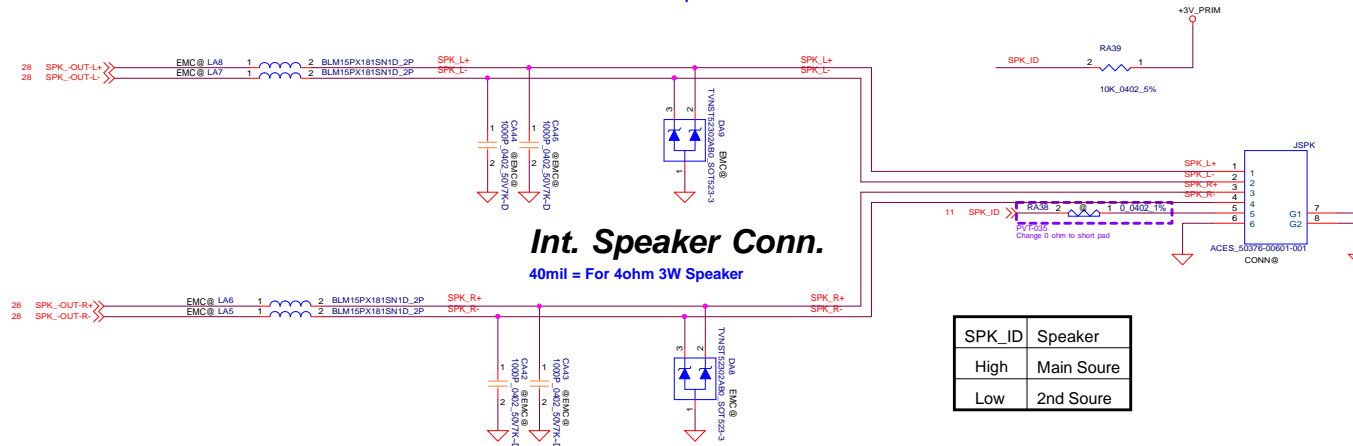
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/10/22	Deciphered Date	2013/10/28	Title	P26-SIM Card CONN
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## Int. Speaker Conn.

40mil = For 4ohm 3W Speaker

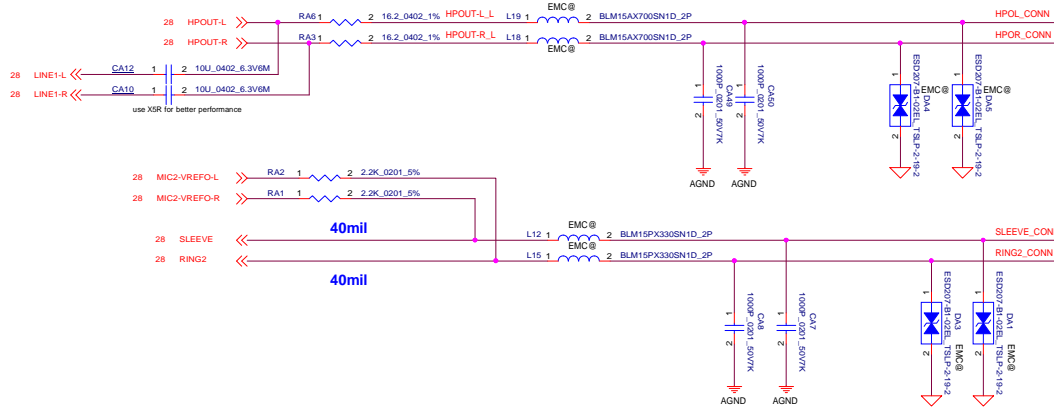


## Int. Speaker Conn.

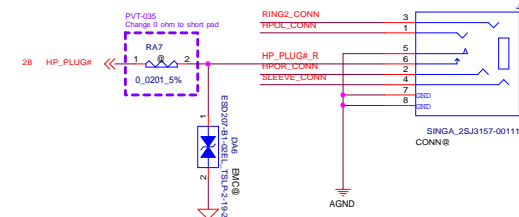
40mil = For 4ohm 3W Speaker

SPK_ID	Speaker
High	Main Soure
Low	2nd Soure

## Universal Audio Jack



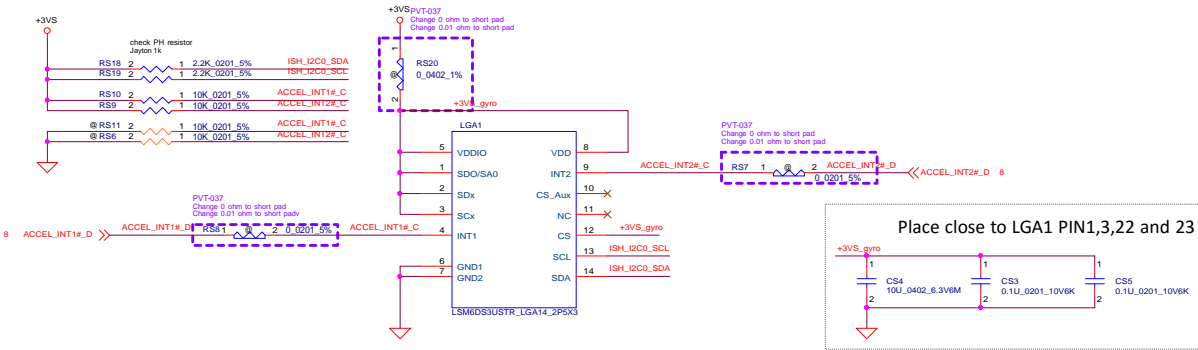
## Universal Audio Jack CONN



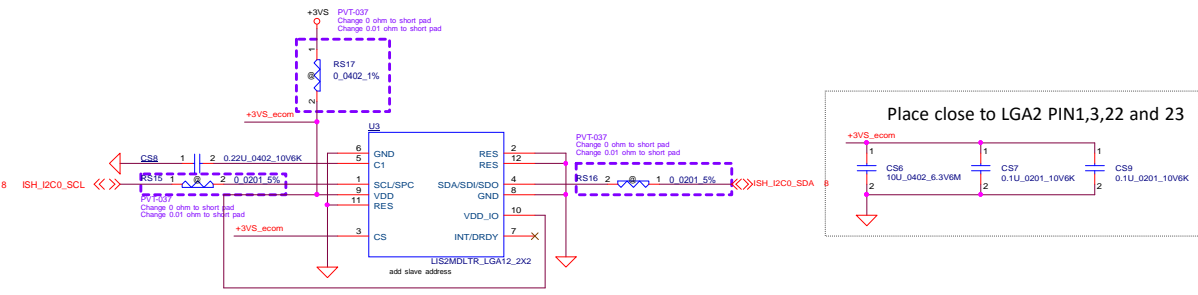




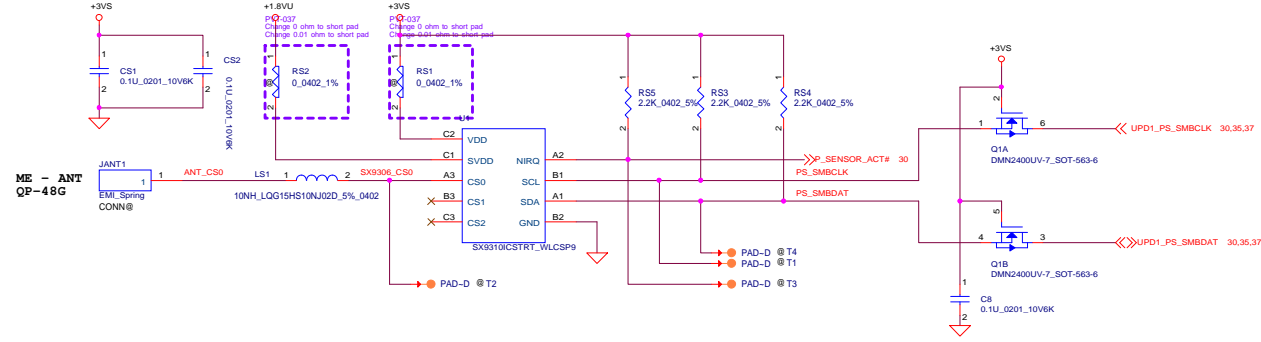
Gyro + Accelerometer



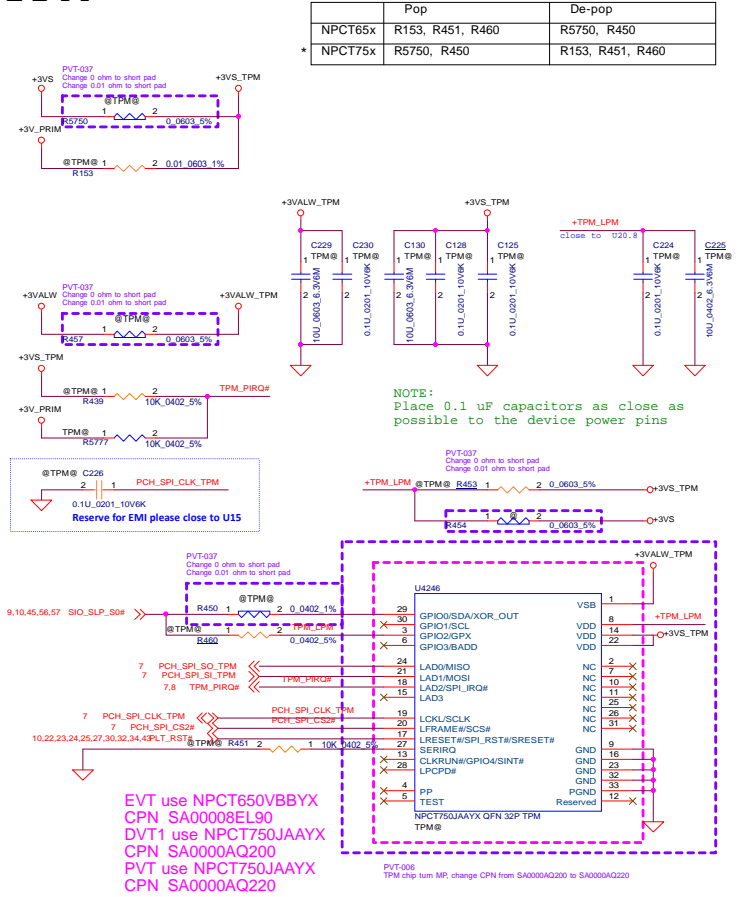
E-Compass

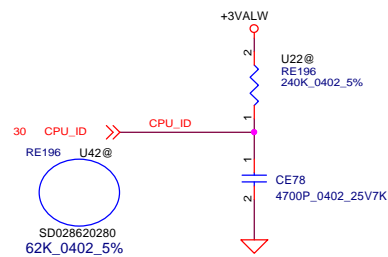
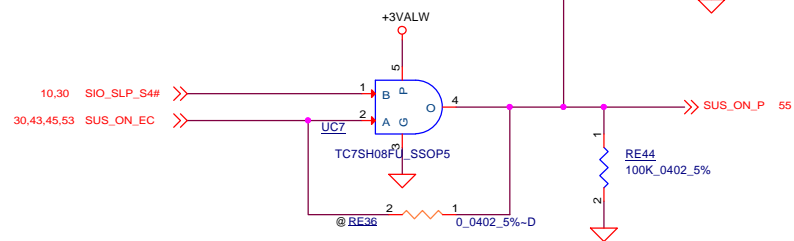
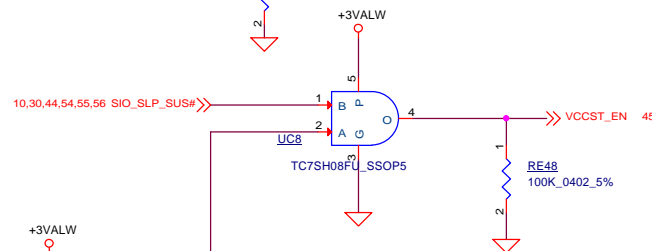
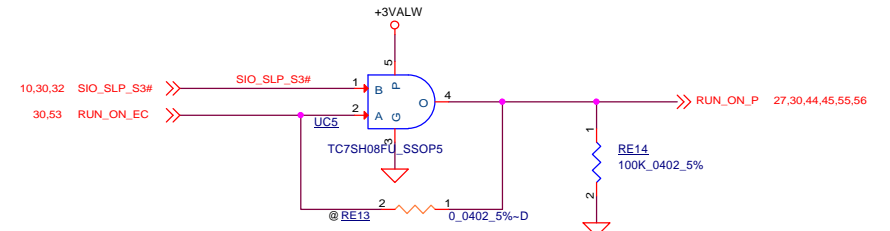
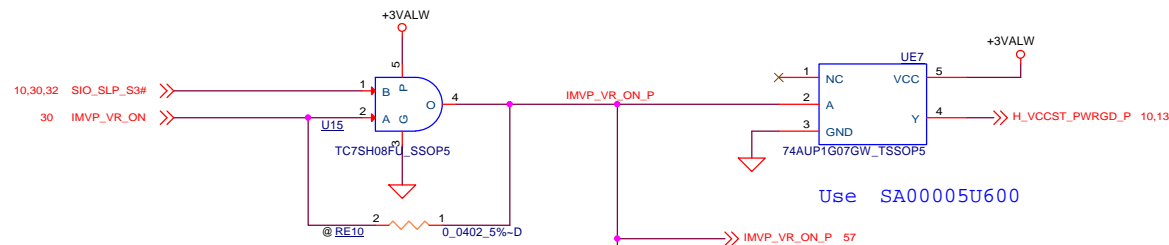
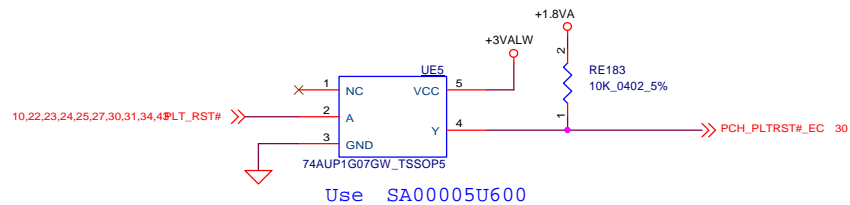


SAR Proximity Sensor

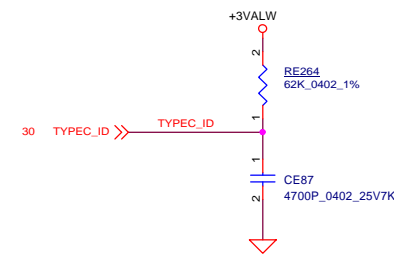


TPM





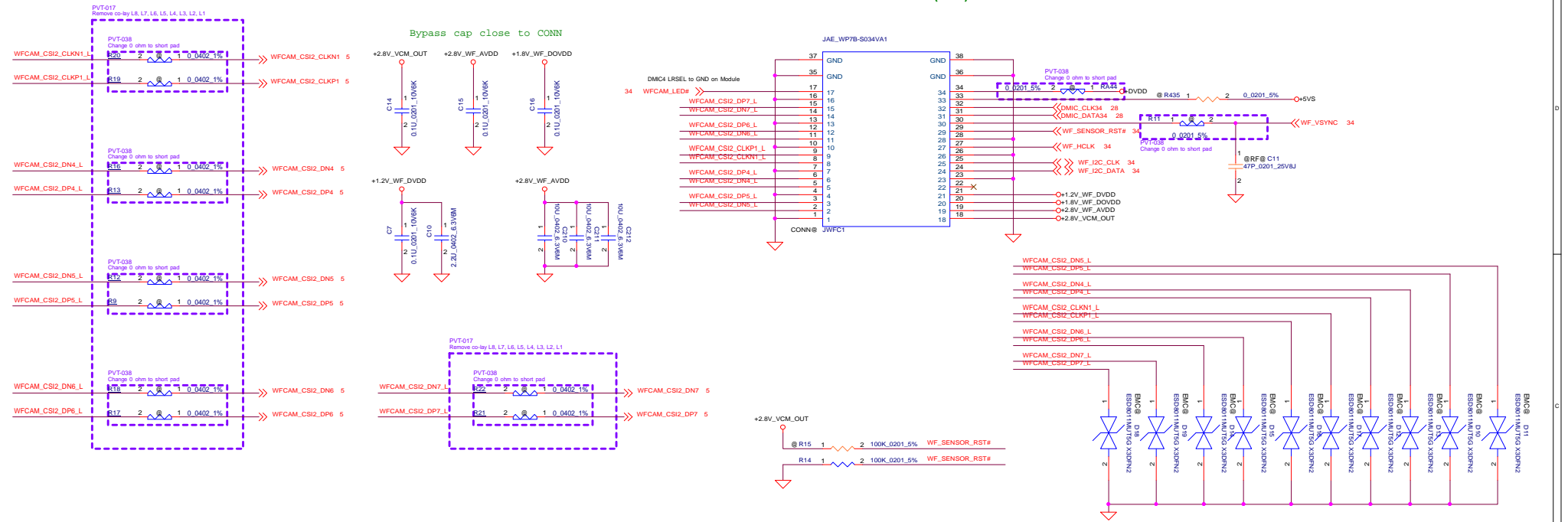
RE196	CE78	REV
240K	4700p	U2+2
130K	4700p	
62K	4700p	U4+2
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	



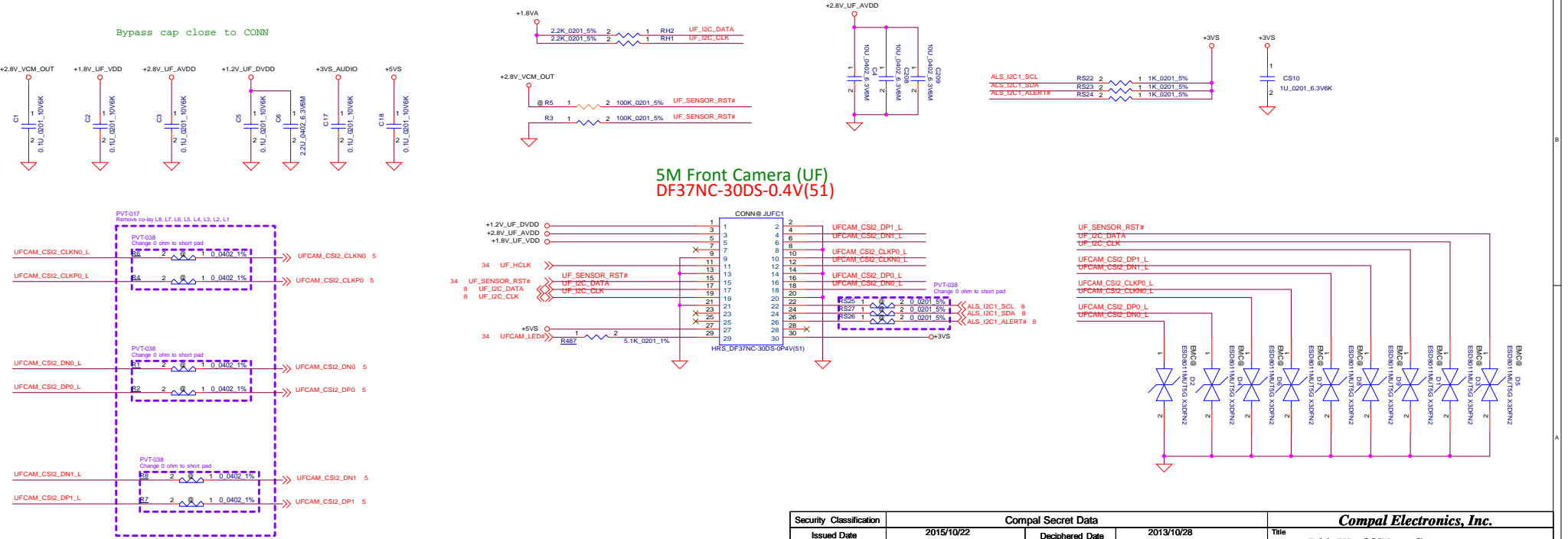
RE264	CE87	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/ AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/ AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

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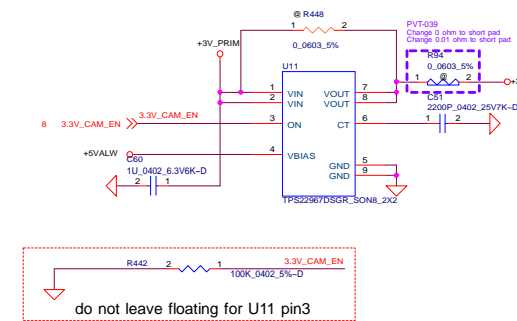
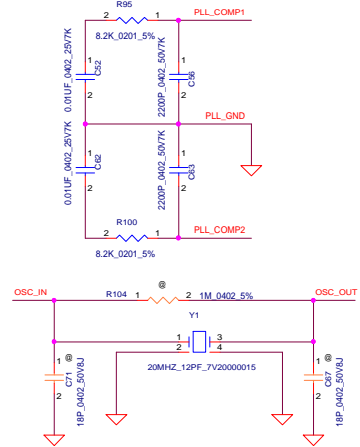
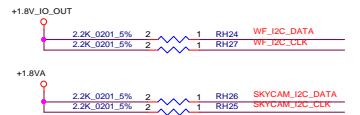
8M Rear Camera (WF)



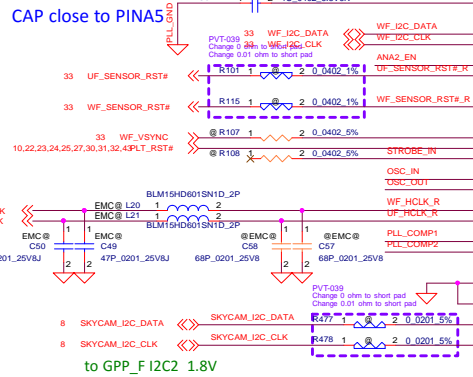
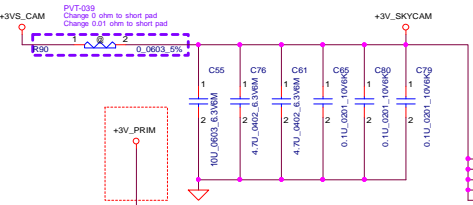
5M Front Camera (UF)  
DF37NC-30DS-0.4V(51)



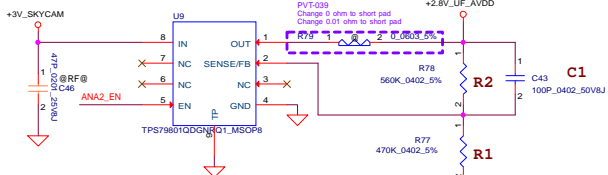
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				Size	Document Number	Rev
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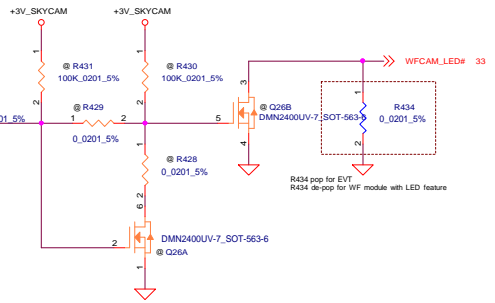
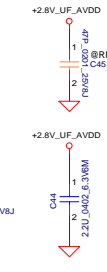
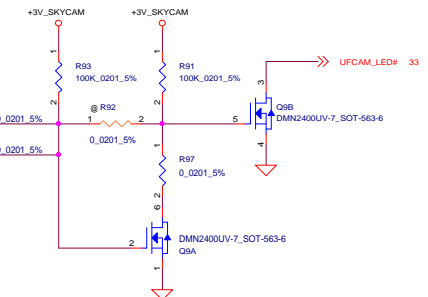
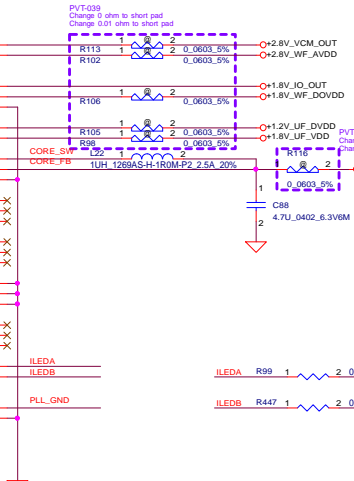
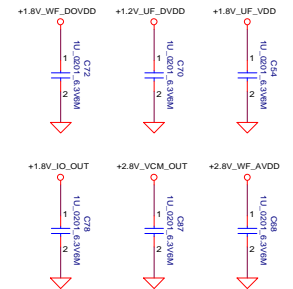
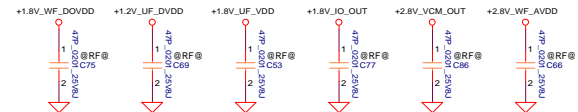
do not leave floating for U11 pin3



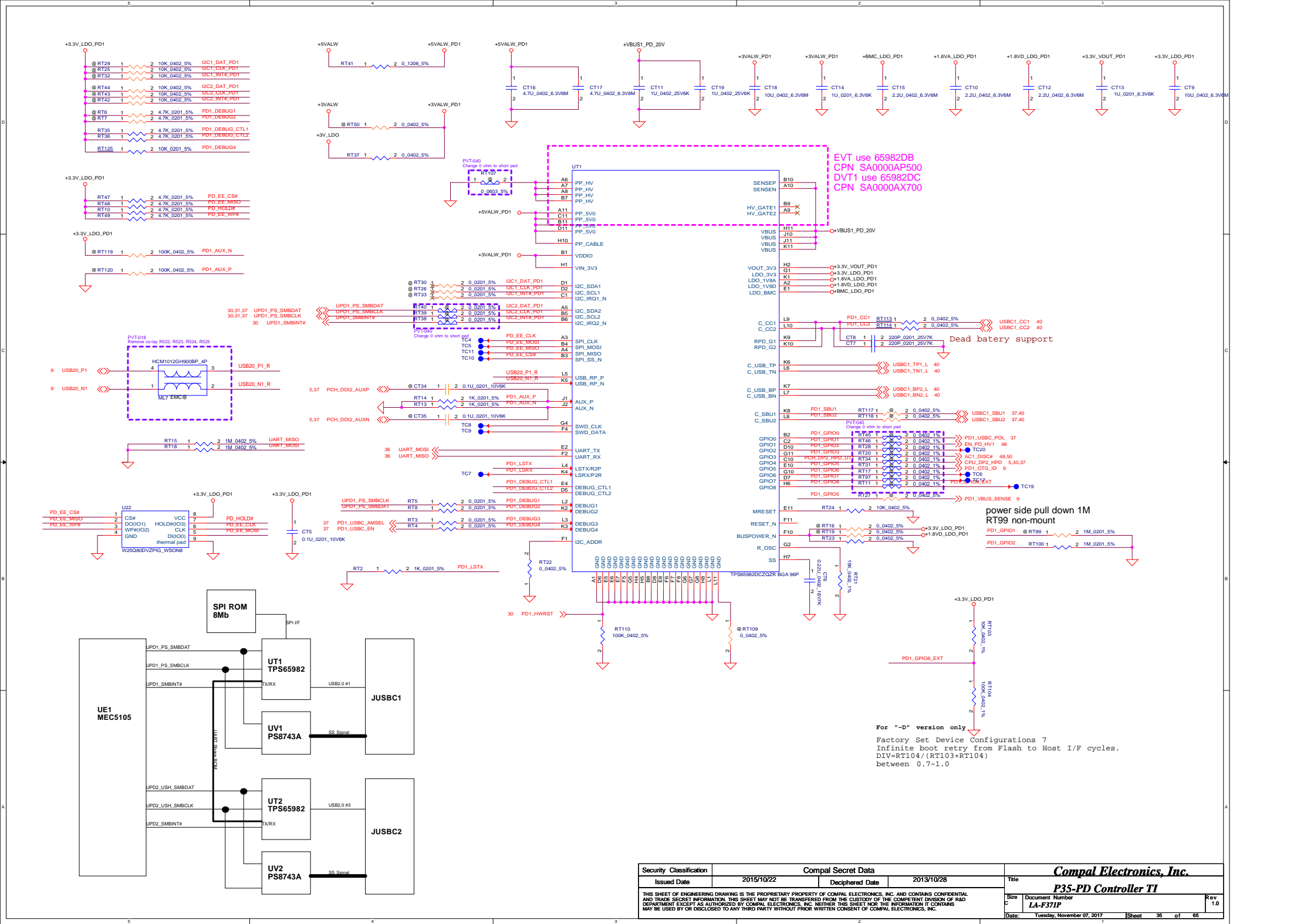
to GPP\_F12C2 1.8V



$V_{OUT} = 1.275 \text{ V} (1 + R2 / R1) + I_{FB} \cdot R2$   
 $V_{FB} = 1.275 \text{ V}$   
 $I_{FB} = 0.53 \mu\text{A at } 25^\circ\text{C}$   
 Output Range = 1.275 V to 28 V  
 A 100-pF capacitor (C1) placed in parallel with R2 of the output divider is necessary



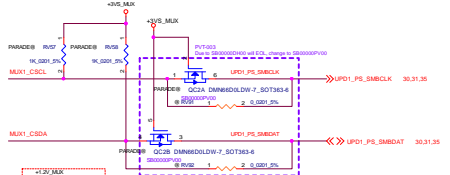
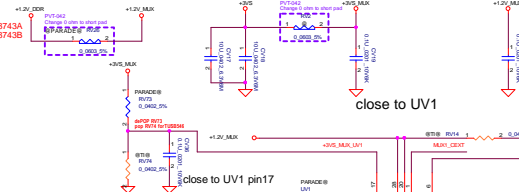
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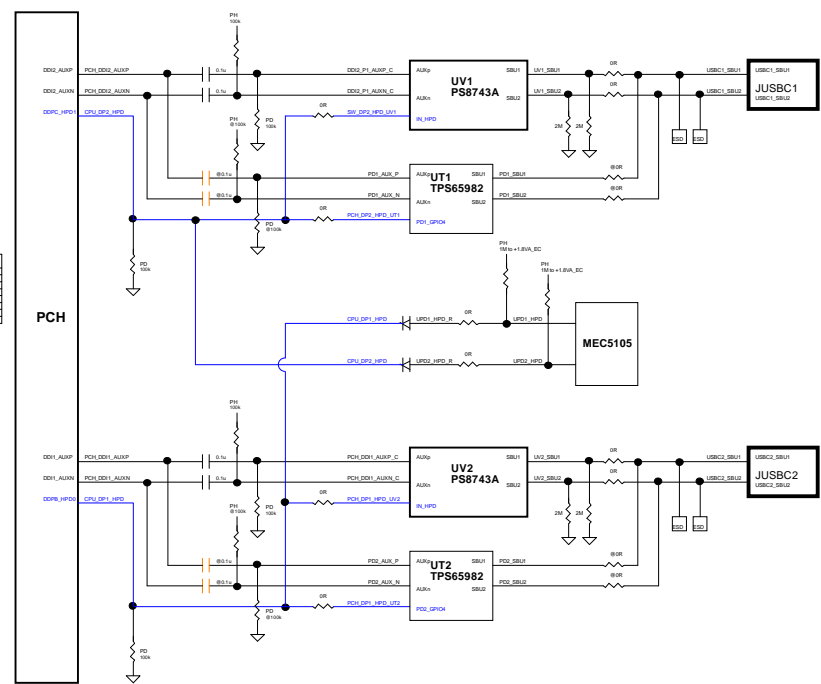
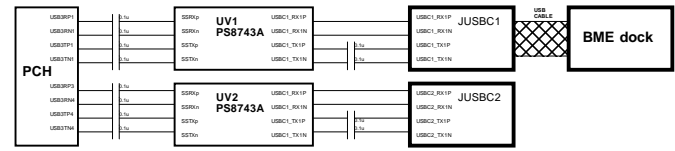
RV26 pop and RV14 de-pop for PS8743A  
RV26 de-pop and RV14 pop for PS8743B



USB1 MUX default H/W setting

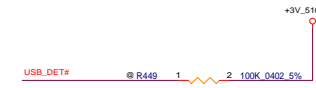
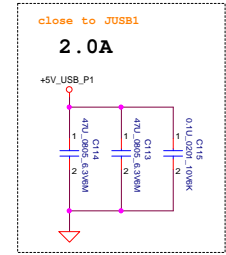
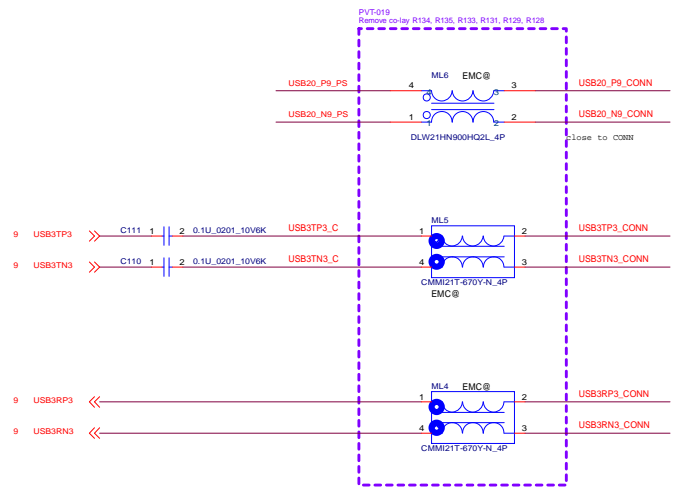
CE_DP	CE_USB	FLTP	USB30E Configuration	USB30E Configuration
L	L	L	Power Mode	Power Mode
L	L	L	USB30E 1.1 - 1.2 VDD	USB30E 1.1 - 1.2 VDD
L	L	L	USB30E 1.1 - 1.2 VDD	USB30E 1.1 - 1.2 VDD
L	L	L	USB30E 1.1 - 1.2 VDD	USB30E 1.1 - 1.2 VDD
L	L	L	USB30E 1.1 - 1.2 VDD	USB30E 1.1 - 1.2 VDD
L	L	L	USB30E 1.1 - 1.2 VDD	USB30E 1.1 - 1.2 VDD
L	L	L	USB30E 1.1 - 1.2 VDD	USB30E 1.1 - 1.2 VDD
L	L	L	USB30E 1.1 - 1.2 VDD	USB30E 1.1 - 1.2 VDD
L	L	L	USB30E 1.1 - 1.2 VDD	USB30E 1.1 - 1.2 VDD
L	L	L	USB30E 1.1 - 1.2 VDD	USB30E 1.1 - 1.2 VDD

USB 3.0 AC Coupling Capacitor Topology



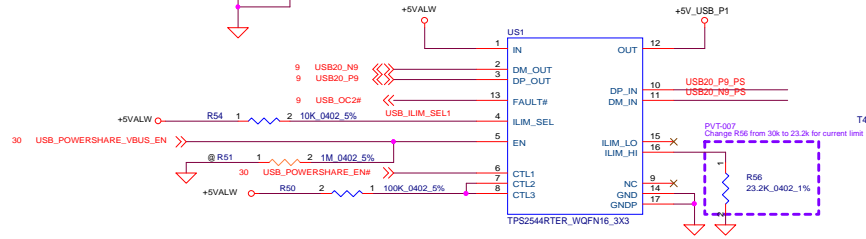
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Issued Date	2015/10/22	Designed Date
2015/10/28		
Rev	1.0	Rev
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Page	1	Page

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2015/10/22	Deciphered Date	2013/10/28	Title	P38-DDI WiGig MUX	
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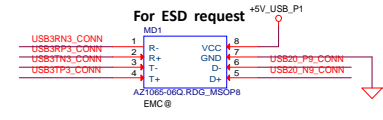
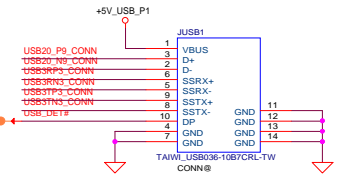
## 2.1A / Channel

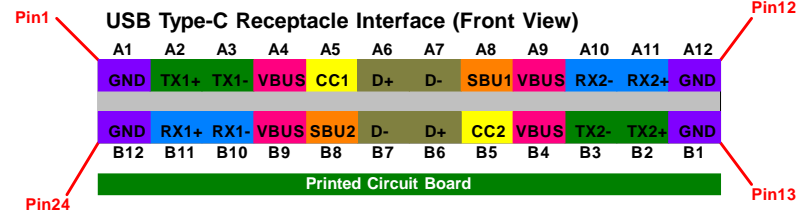
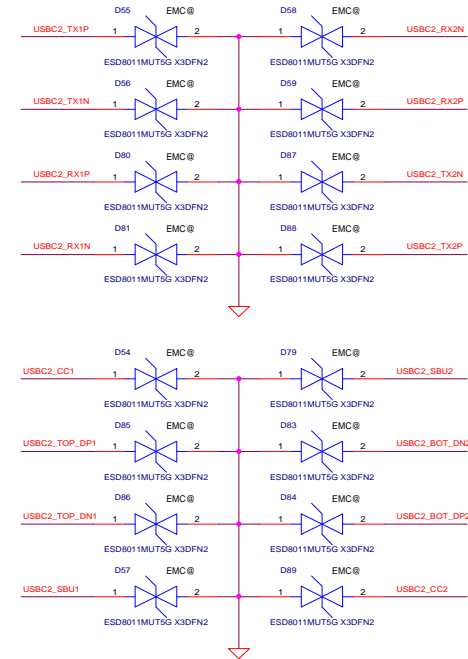
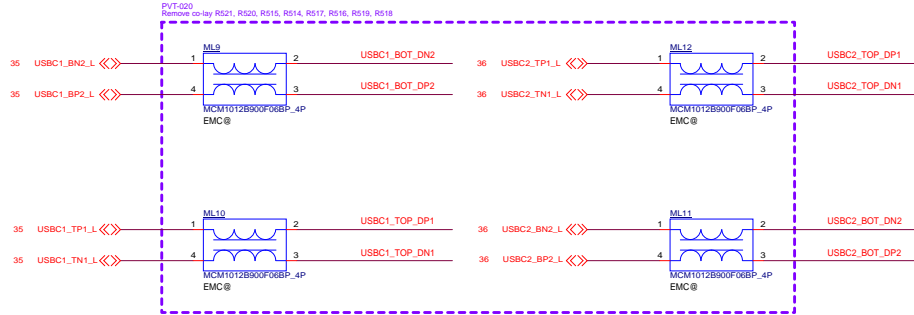
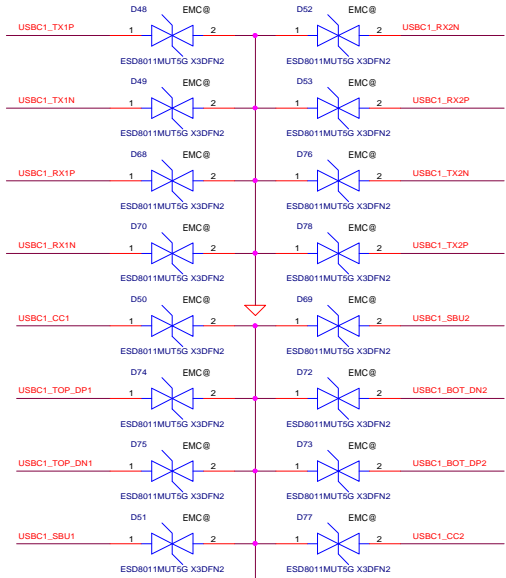
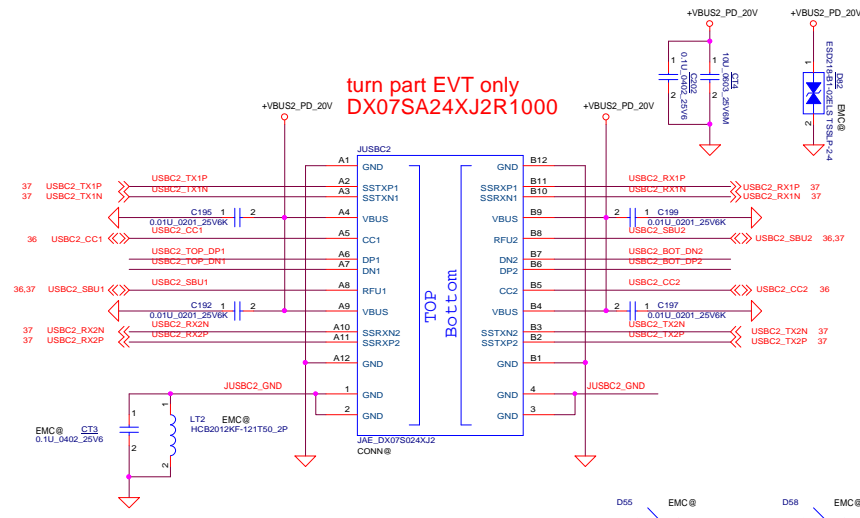
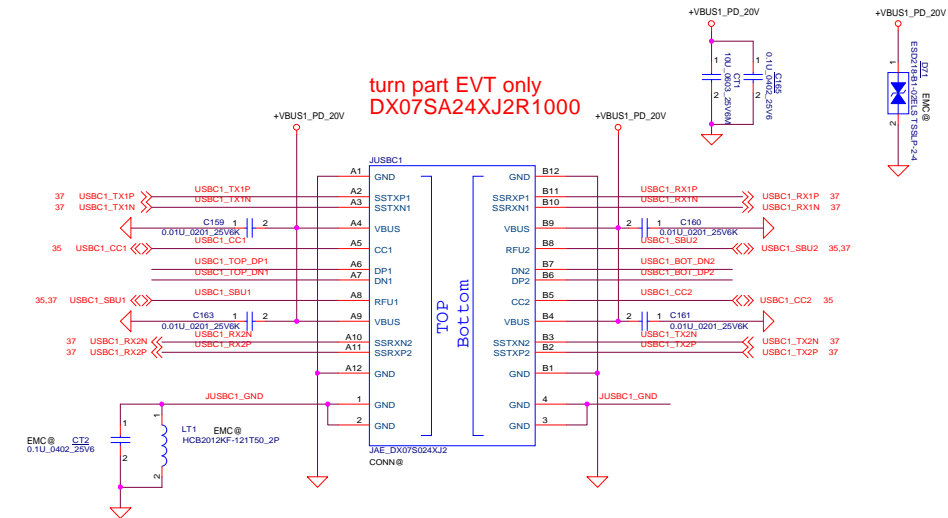
### USB Power Share



CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP

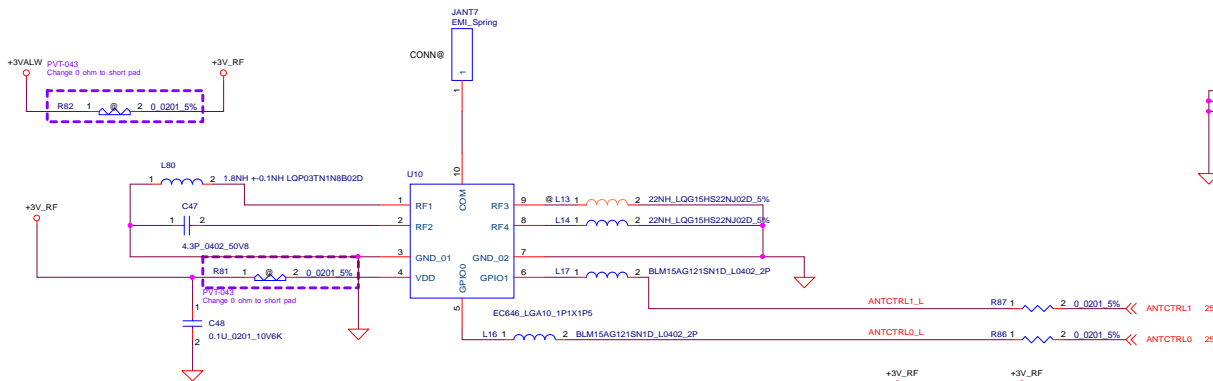
### USB TYPE-A CONN





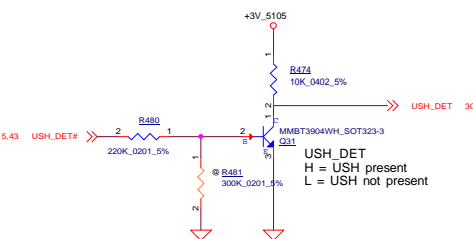
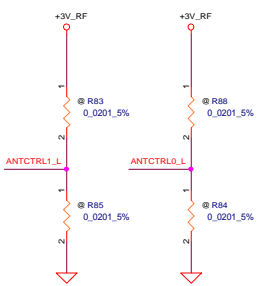
Tunable IC

RF conn for WWAN

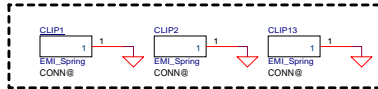
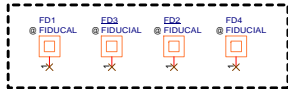


Truth Table

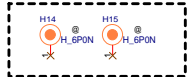
GPIO0	GPIO0	RF1	RF2	RF3	RF4
L	L	ON	OFF	OFF	OFF
L	H	OFF	ON	OFF	OFF
H	L	OFF	OFF	ON	OFF
H	H	OFF	OFF	OFF	ON



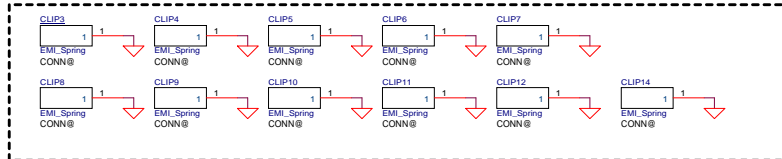
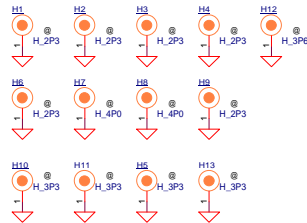
## SCREW HOLE



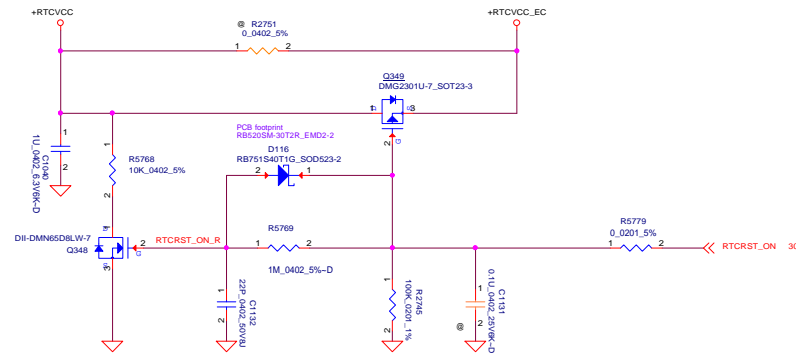
for cable routing



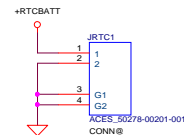
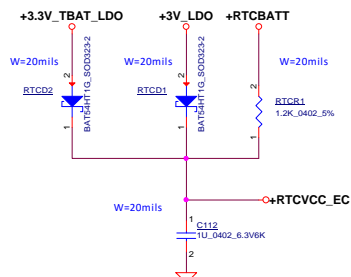
for WLAN/WWAN



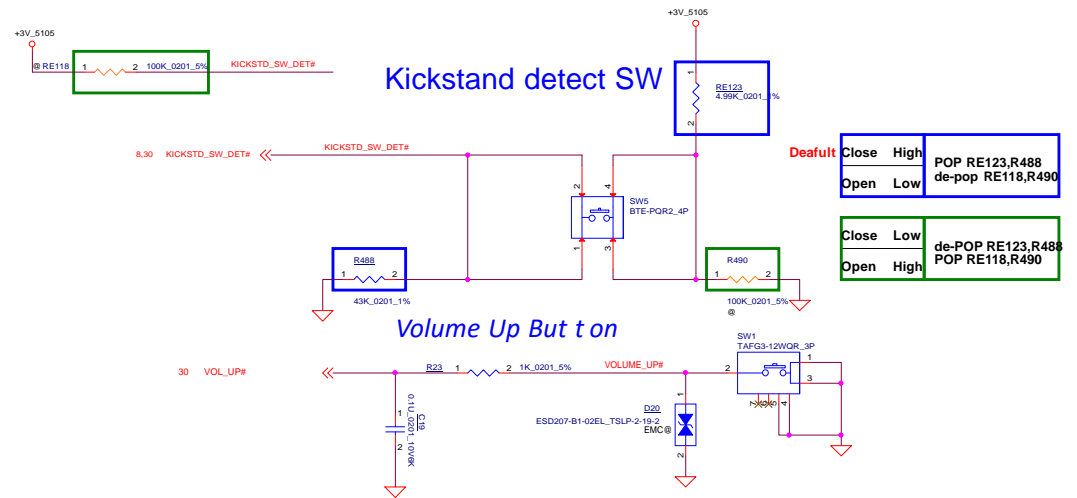
for M.2 SSD/WLAN/WWAN shielding clip



## RTC



## Kickstand detect SW



Volume Up But t on

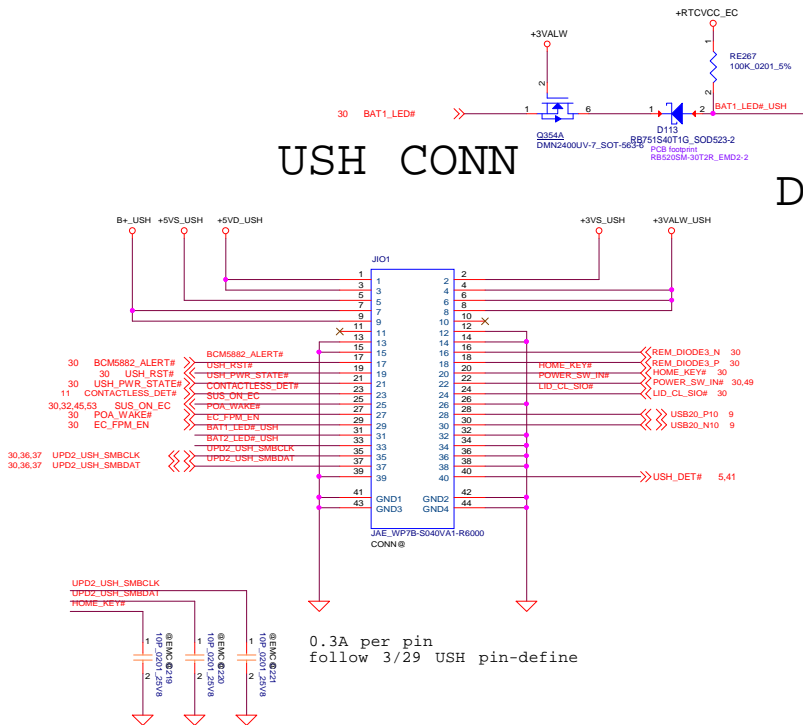
Volume Down But t on

PU 10K resistor locate on EC side

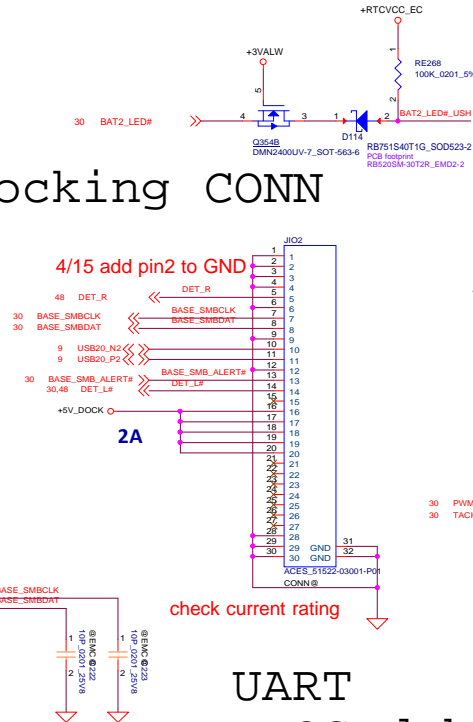
## SATA LED

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				Rev	1.0

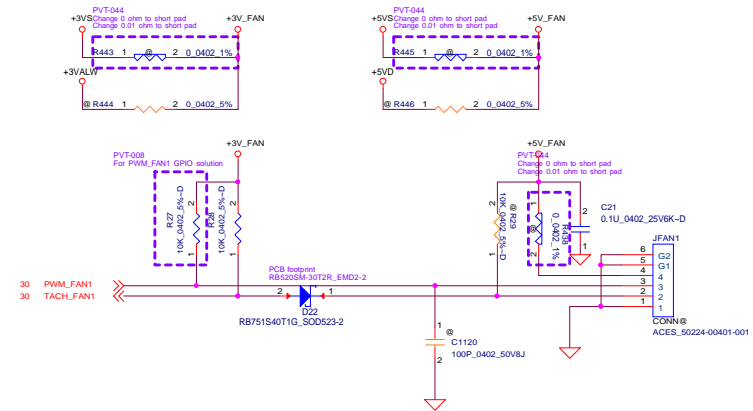
## USH CONN



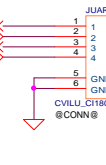
## Docking CONN



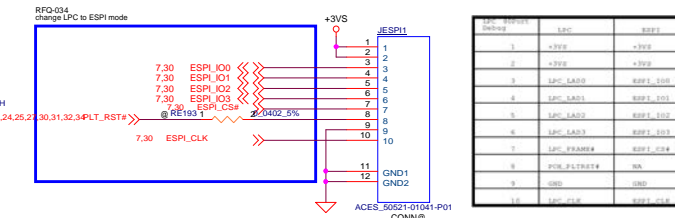
## FAN CONN



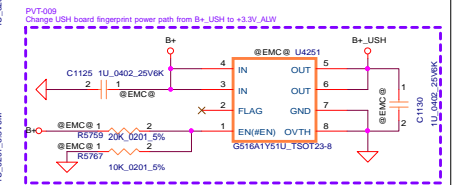
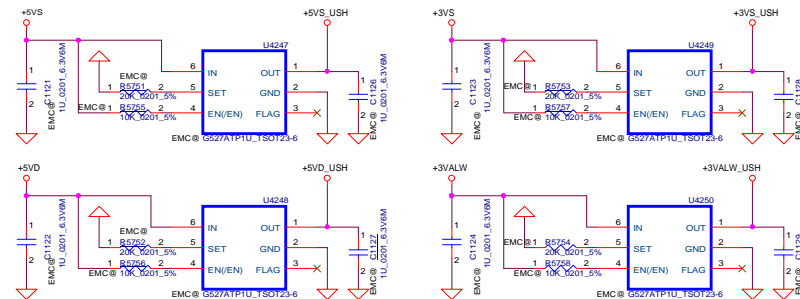
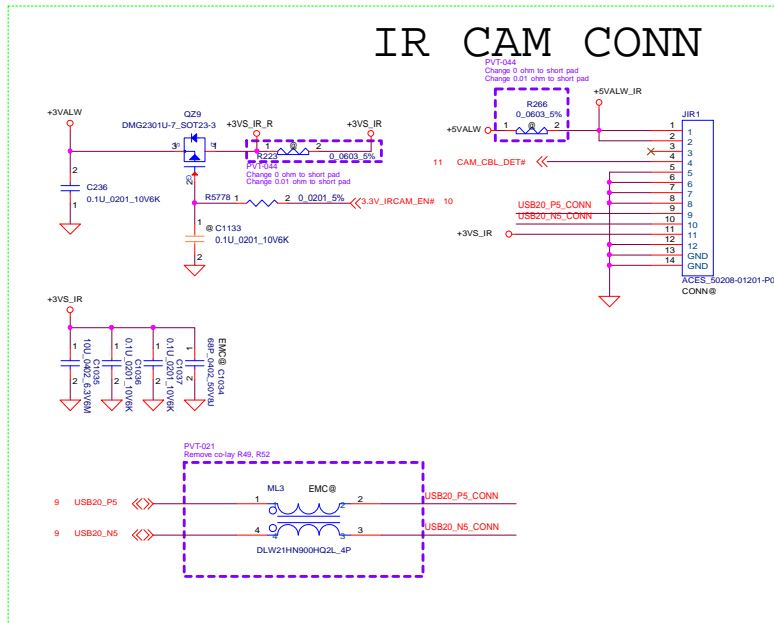
## UART BIOS debug



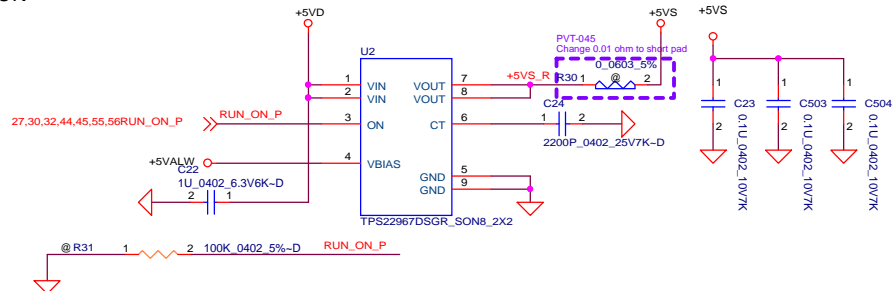
## ESPI BIOS debug



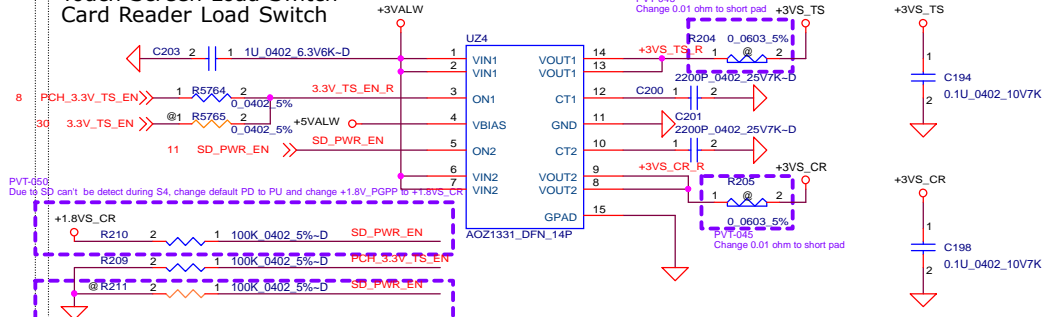
## IR CAM CONN



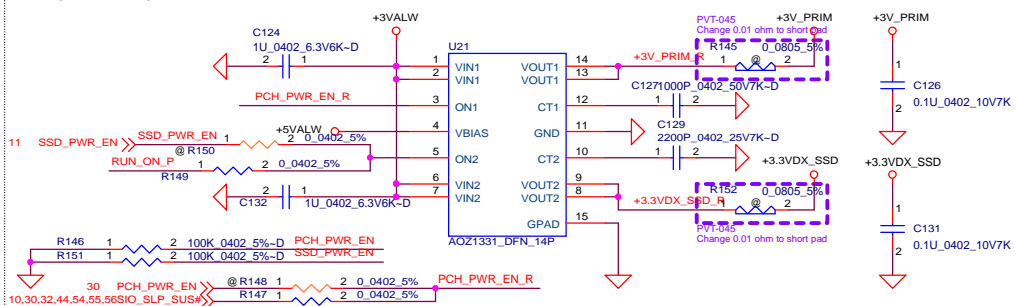
## +5V RUN



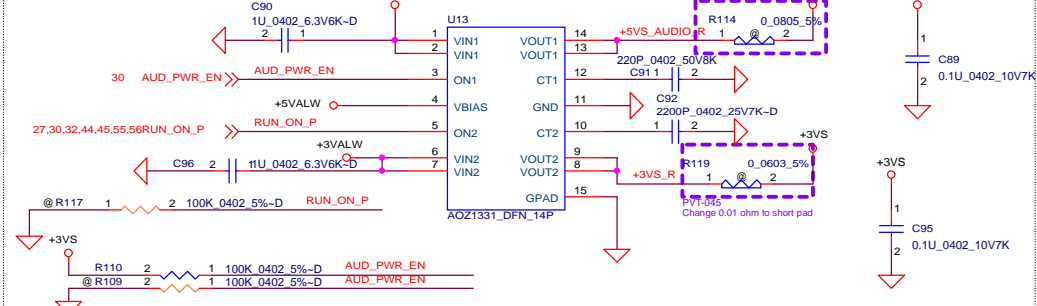
## Touch Screen Load Switch Card Reader Load Switch



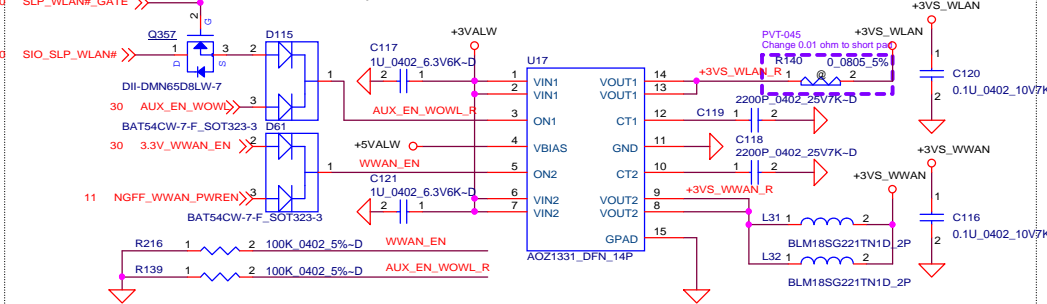
## Deeper Sleep, SSD Load Switch



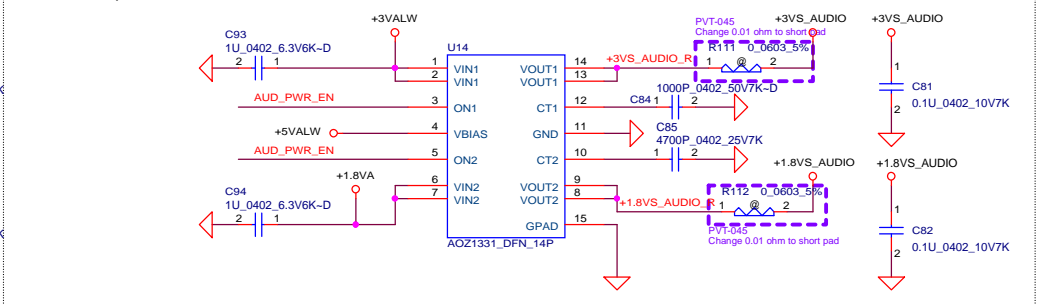
## +5V Audio , 3V Run



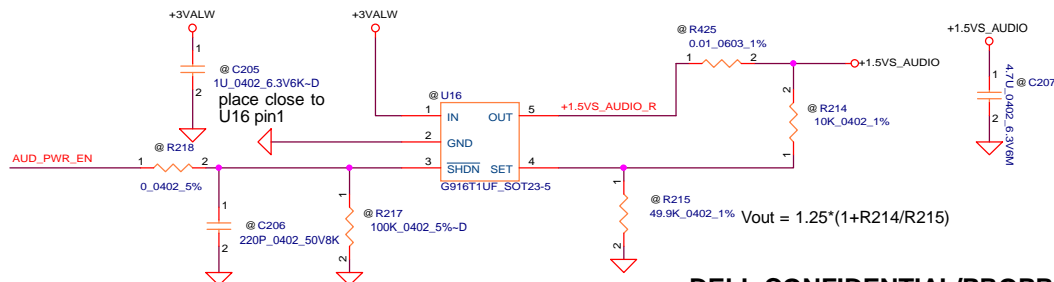
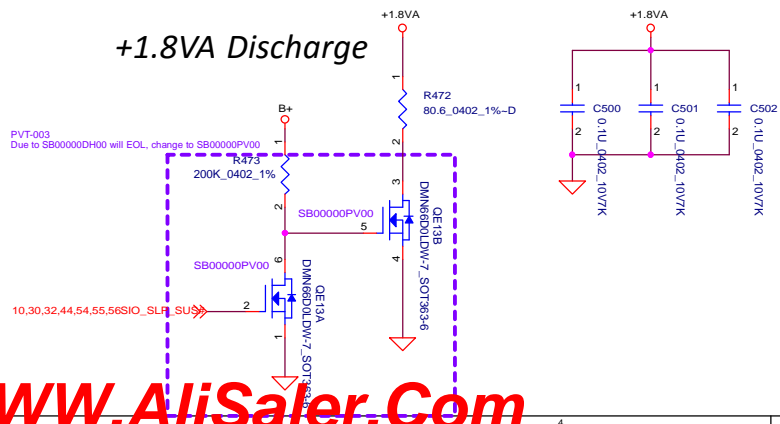
## WLAN/WWAN Load Switch



## 3V\_Audio, 1.8V\_Audio Load Switch



## +1.8VA Discharge



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						Size	
						Document Number	
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						Sheet	
						44 of 65	

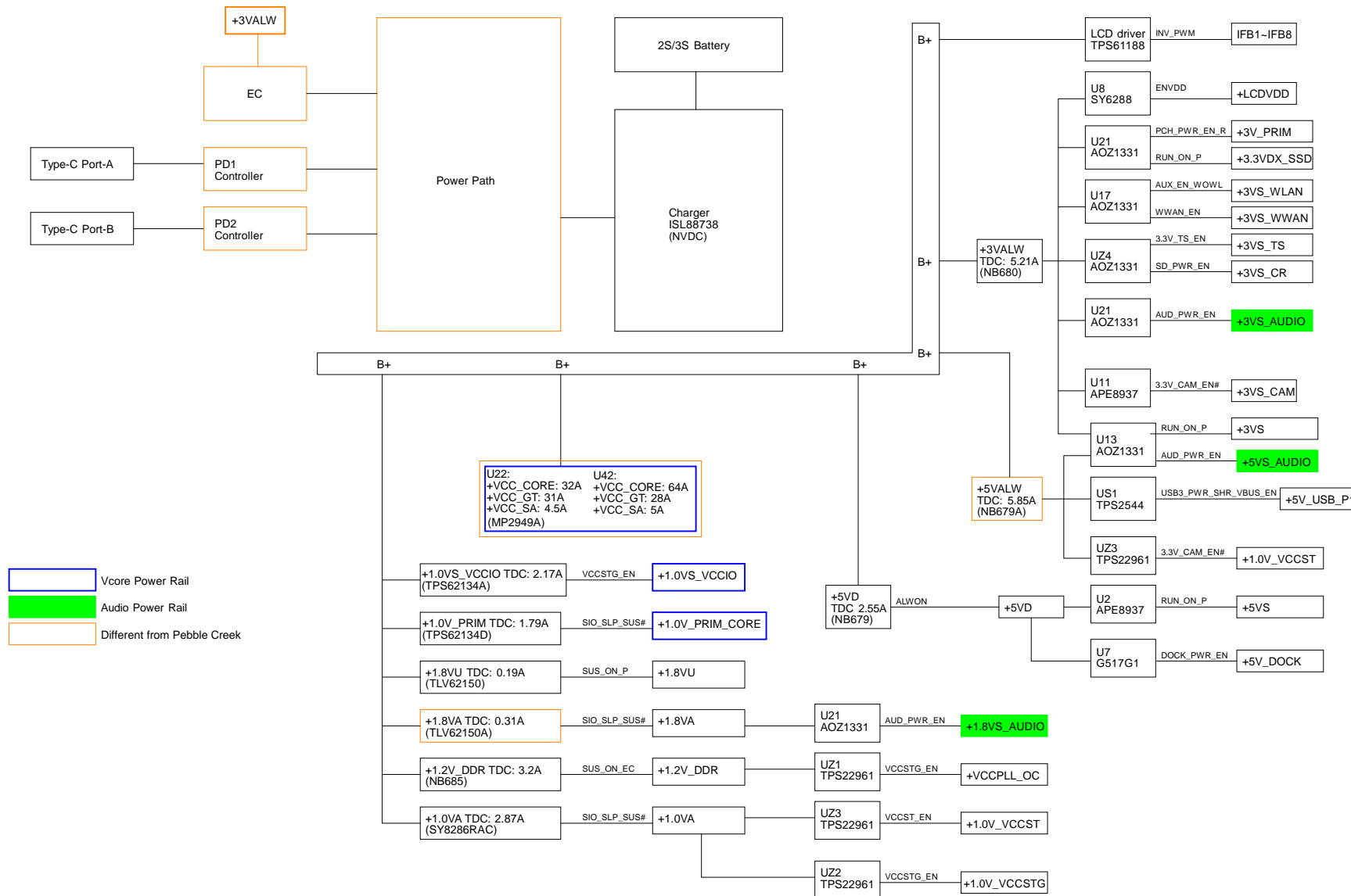
DELL CONFIDENTIAL/PROPRIETARY  
Compal Electronics, Inc.



Title				P44-DC/DC Interface 1			
Size		Document Number		LA-F371P		Rev 1.0	
Date		Tuesday, November 07, 2017		Sheet		44 of 65	



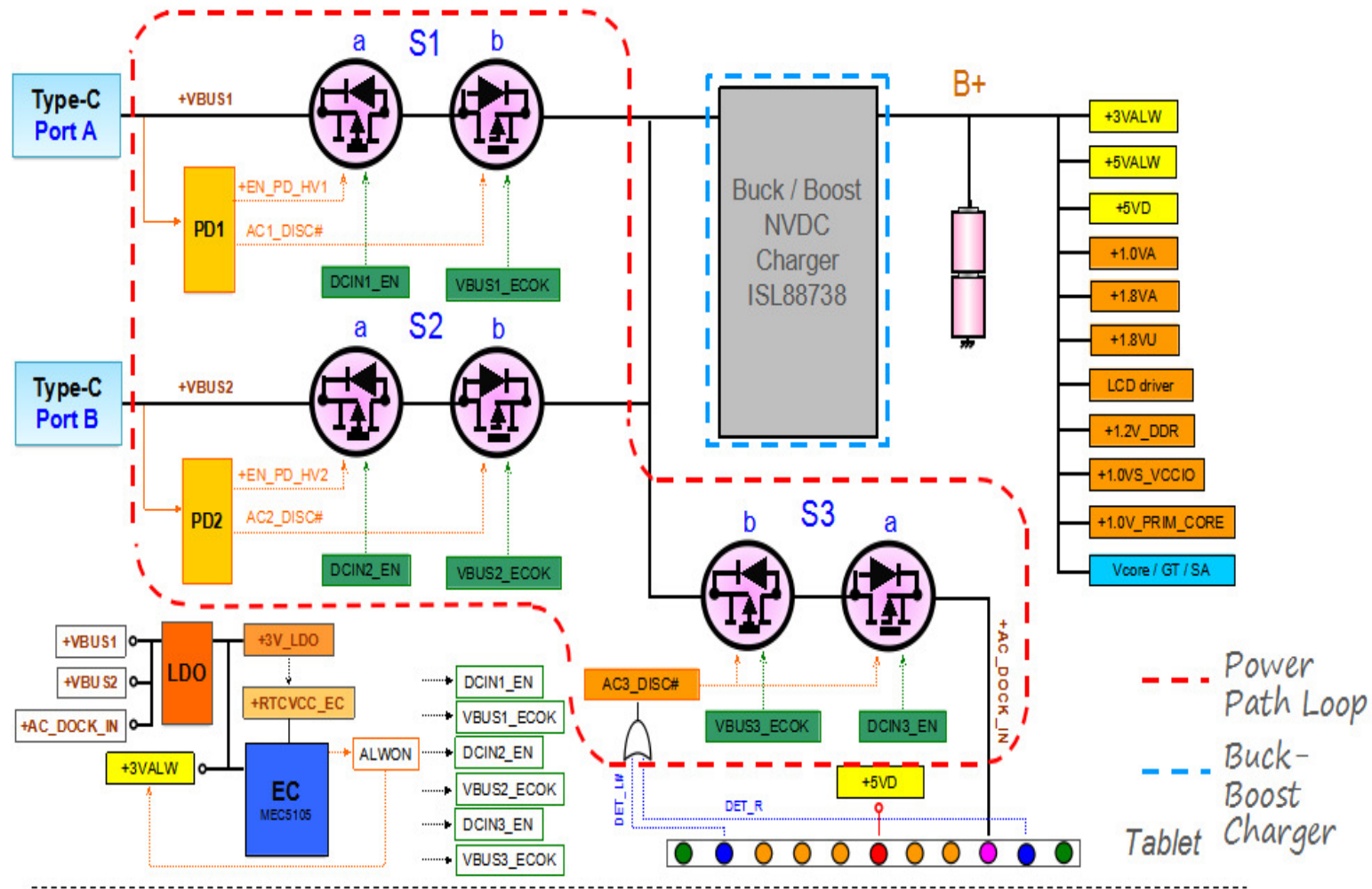


## *Pebble Creek MLK Power Block - Tablet*

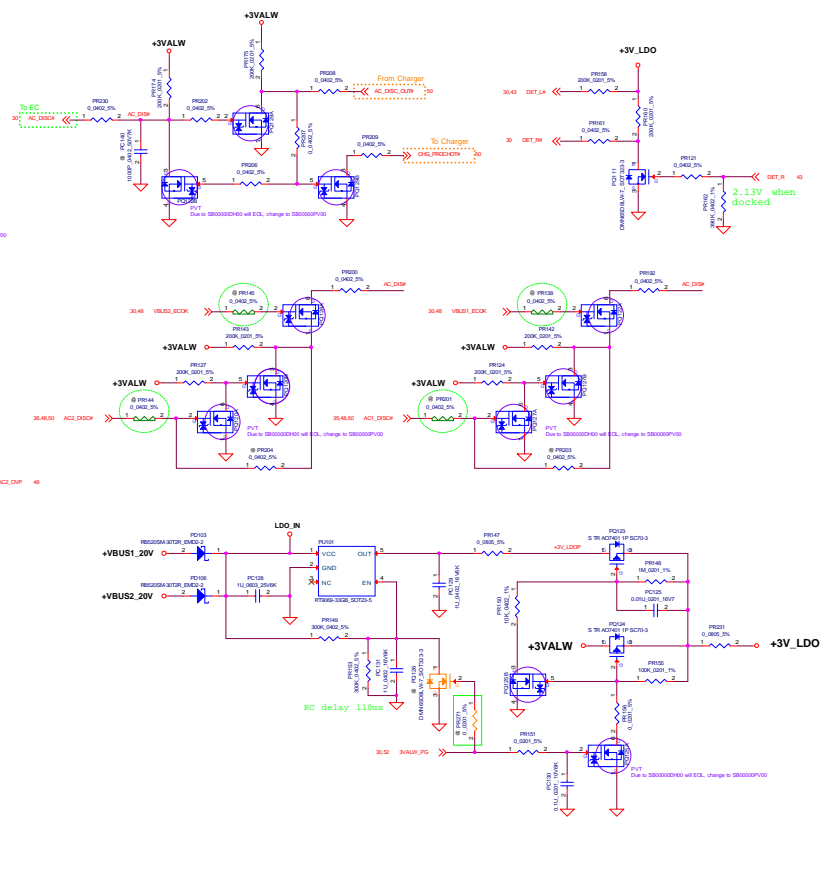
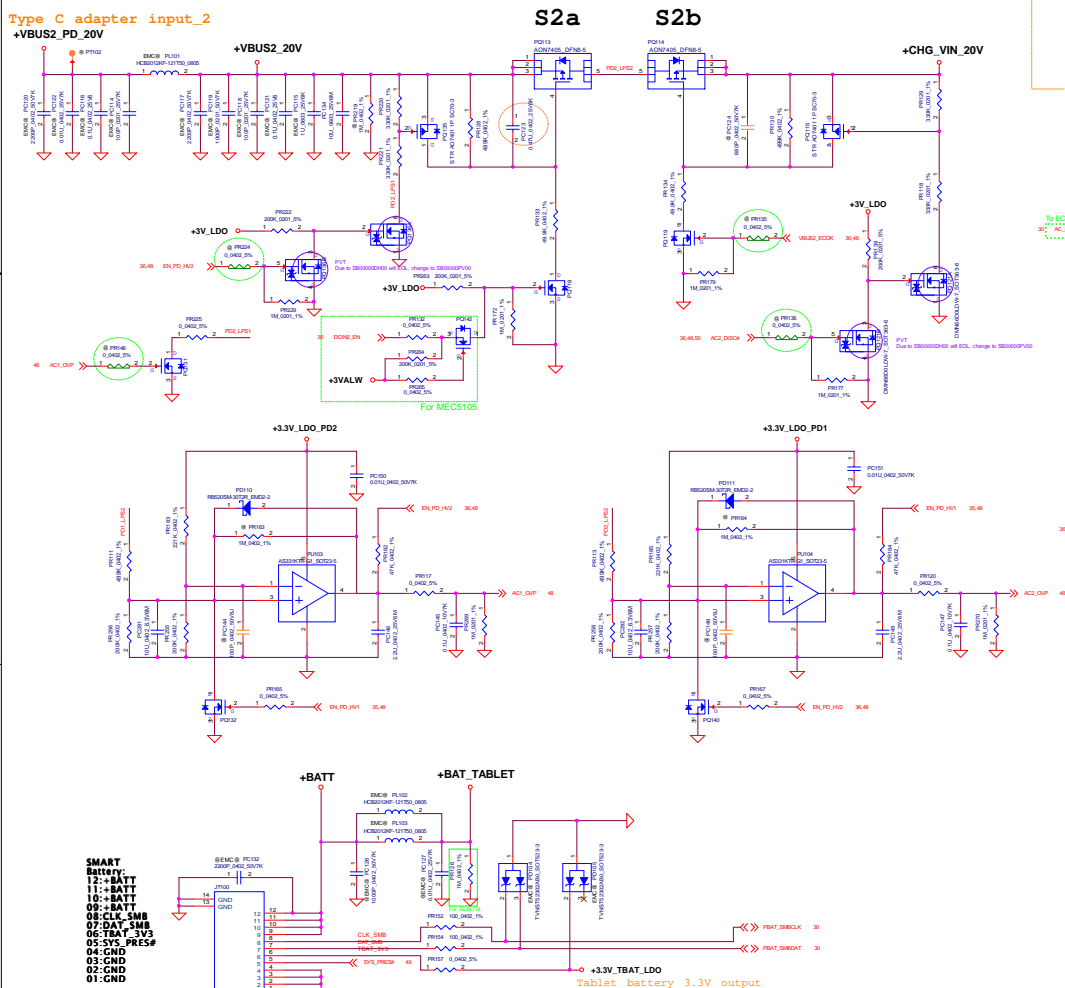
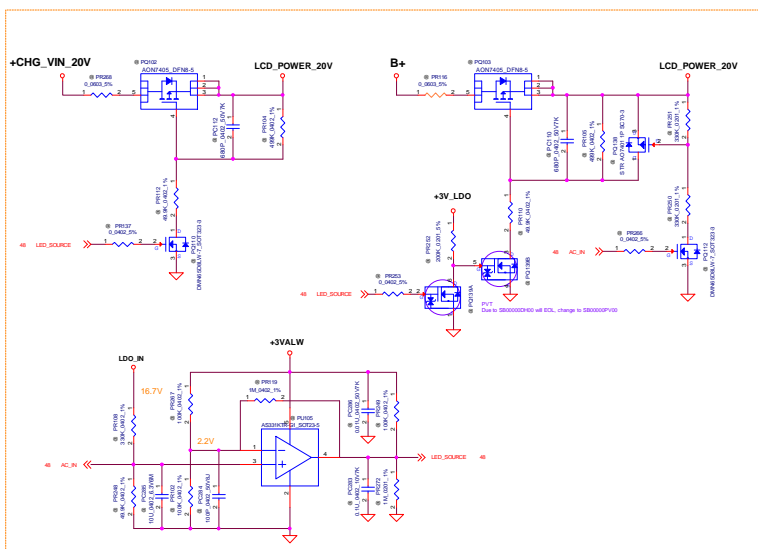
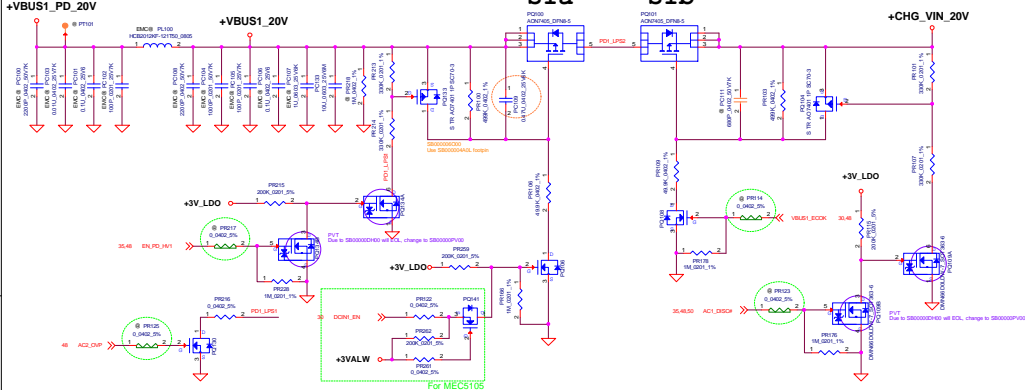


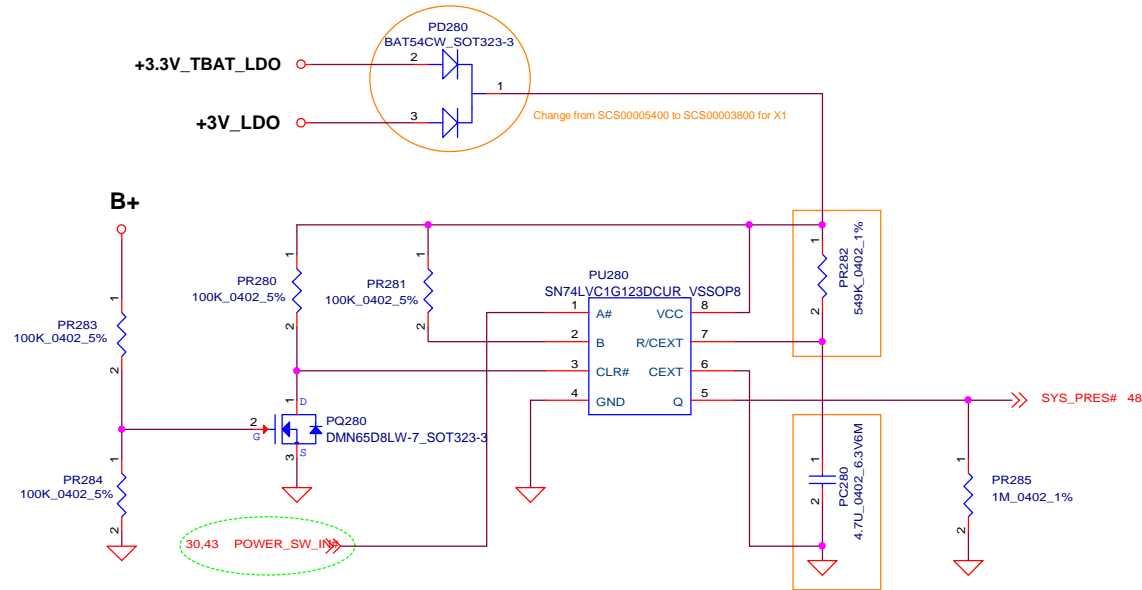
Security Classification	Compel Secret Data		<div>  <b>Compel Electronics, Inc.</b> </div>	
Issued Date	2014/06/20	Deciphered Date	2015/06/20	<div>  <b>PWR POWER BLOCK DIAGRAM</b> </div>
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AND BE SO OR DISCLOSED TO ANY THIRD PARTY WITHOUT WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			001	1.0
Date Issued: November 09, 2017			Rev	00

Pebble Creek MLK Power Path Block



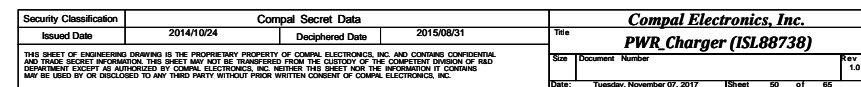
Type C adapter input\_1





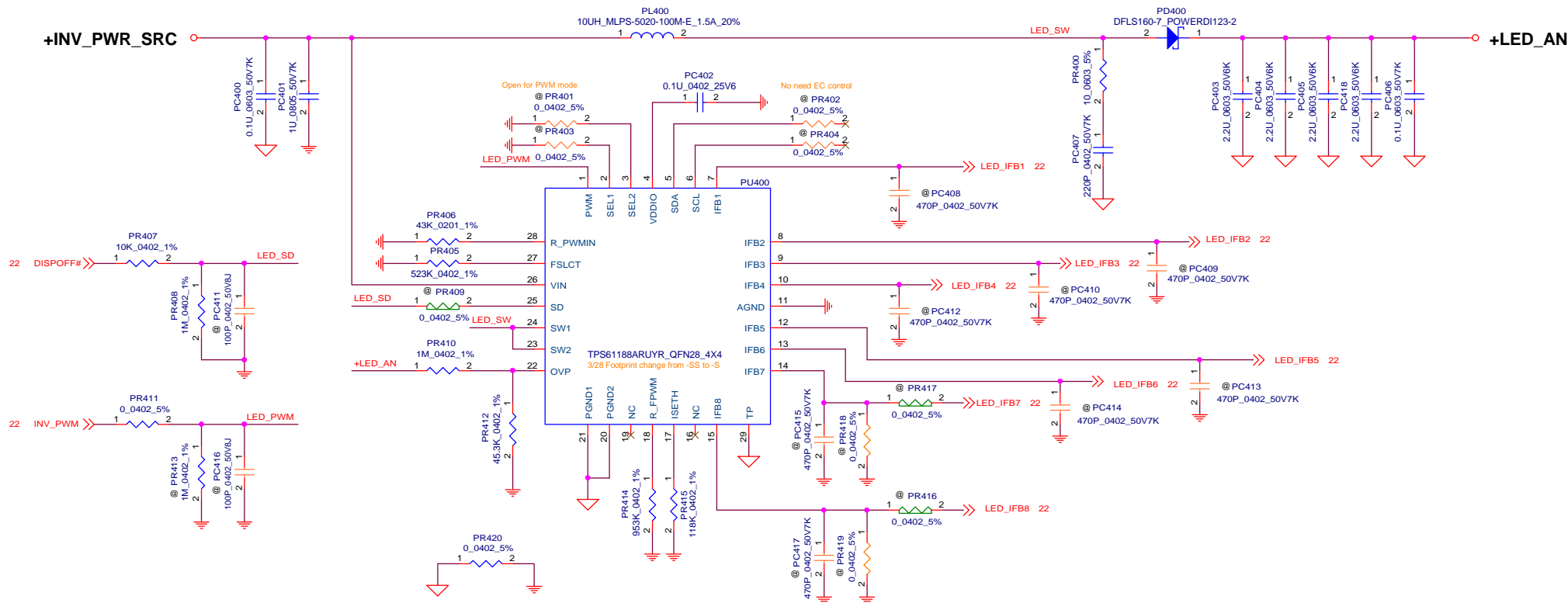
FUNCTION TABLE

INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L <sup>(1)</sup>
X	X	L	L <sup>(1)</sup>
H	L	↑	⌋
H	↓	H	⌋
↑	L	H	⌋



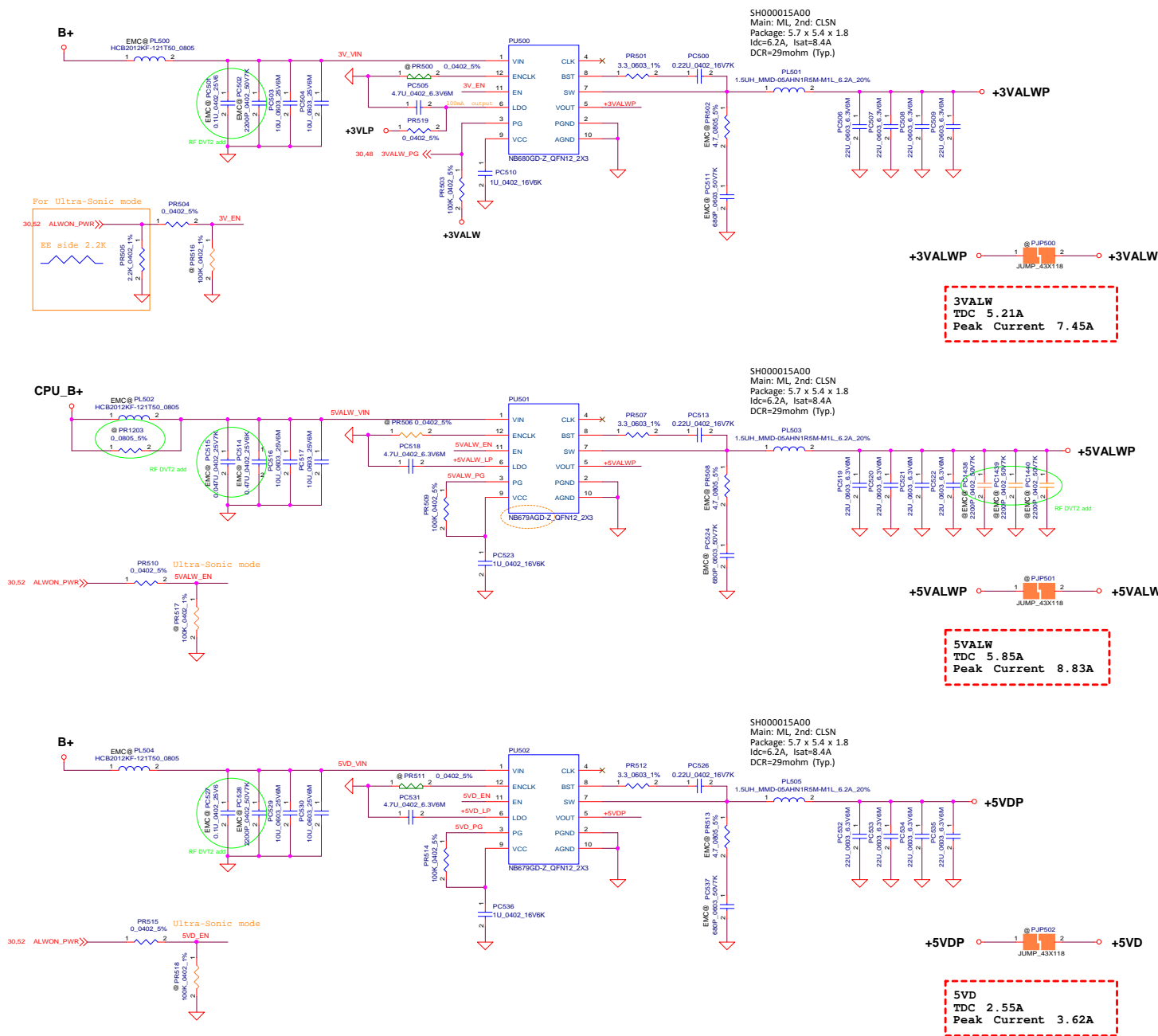
LCD driver controller(35.31), Support component(35.32)

Current:  $11.1\text{mA} \times 8 = 88.8\text{mA}$   
Max Voltage:  $6.2\text{V} \times 6 = 37.2\text{V}$



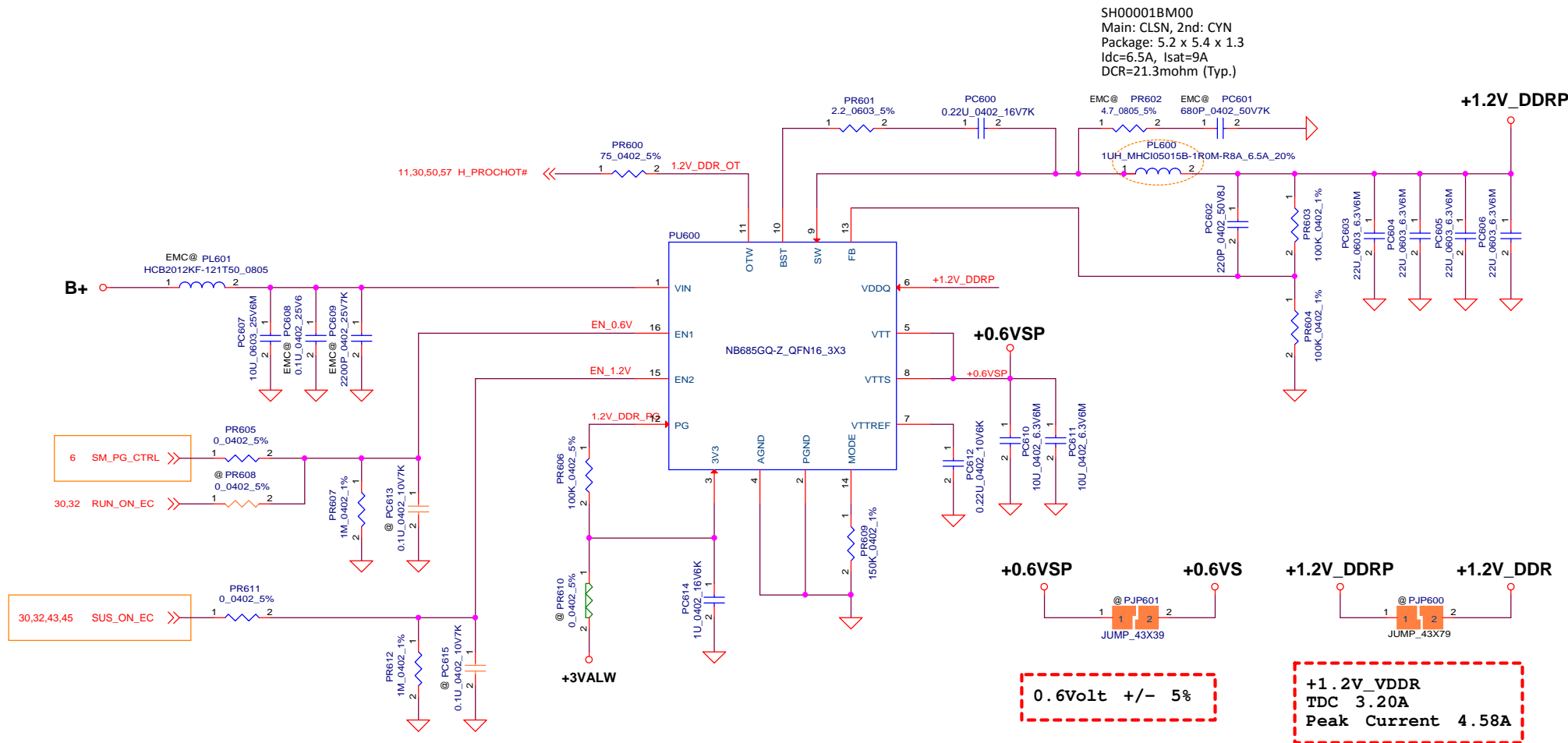
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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				Rev	
				1.0	
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				Sheet 51 of 65	

3V/5V controller(35.1), Support component(35.2)





+1.2V\_DDR controller(35.3), Support component(35.4)

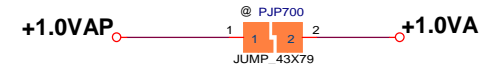


0.6V<sub>olt</sub> +/- 5%

+1.2V\_VDDR  
TDC 3.20A  
Peak Current 4.58A

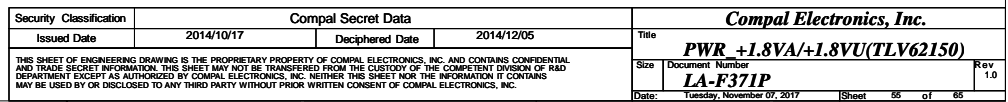
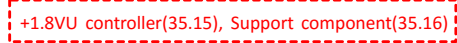
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2013/04/10	Deciphered Date	2014/05/01	Title	
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+1.0VA controller(35.5), Support component(35.6)

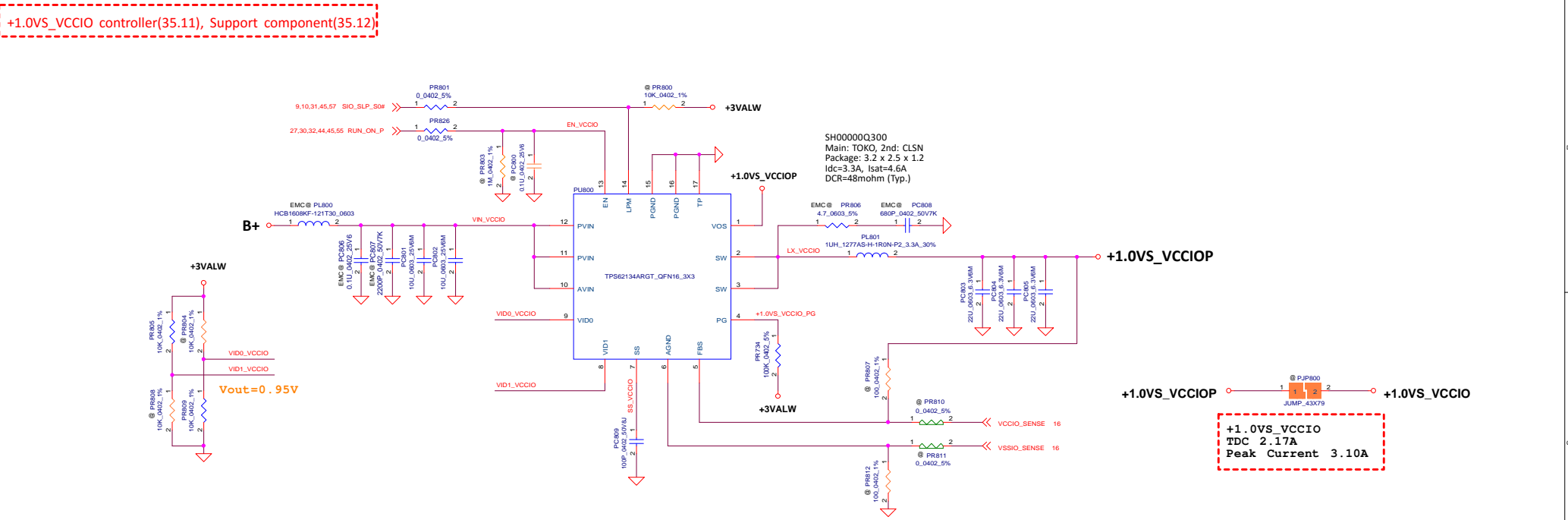


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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title		
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				Size	Document Number	Rev
				<b>LA-F371P</b>		1.0
Date: Tuesday, November 07, 2017				Sheet	54	of 65

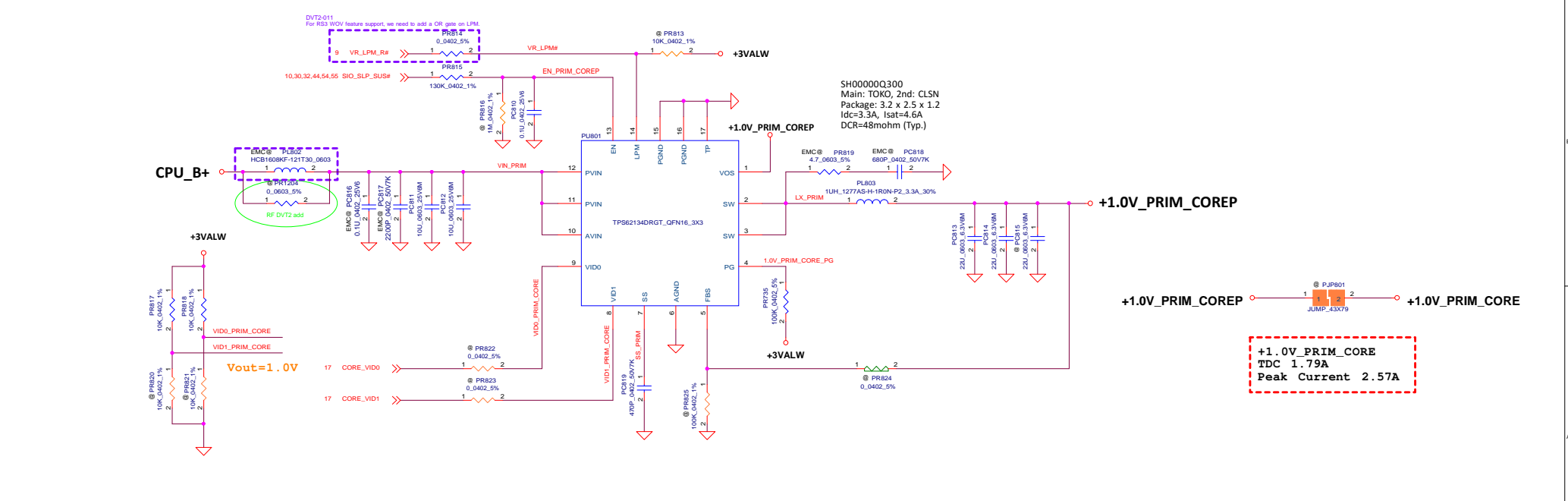
+1.8VS controller(35.13), Support component(35.14)



+1.0VS\_VCCIO controller(35.11), Support component(35.12)

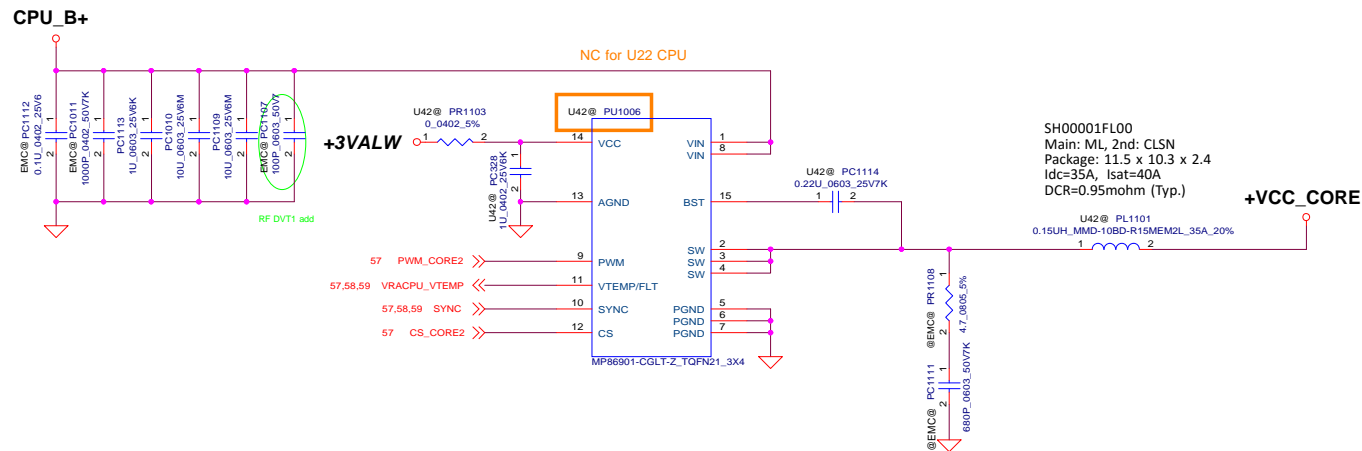


+1.0V\_PRIM\_CORE controller(35.7), Support component(35.



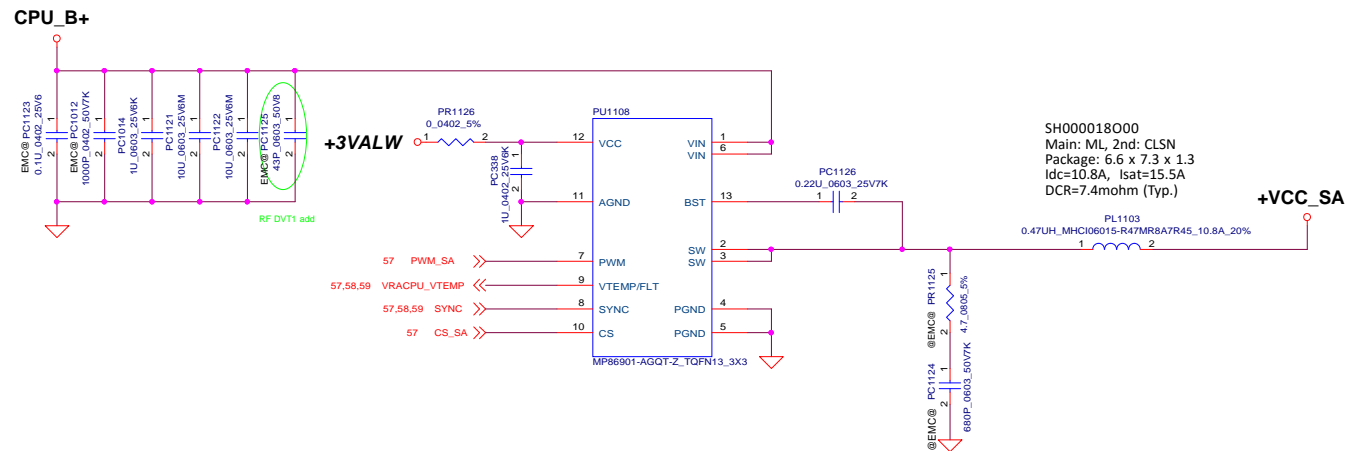
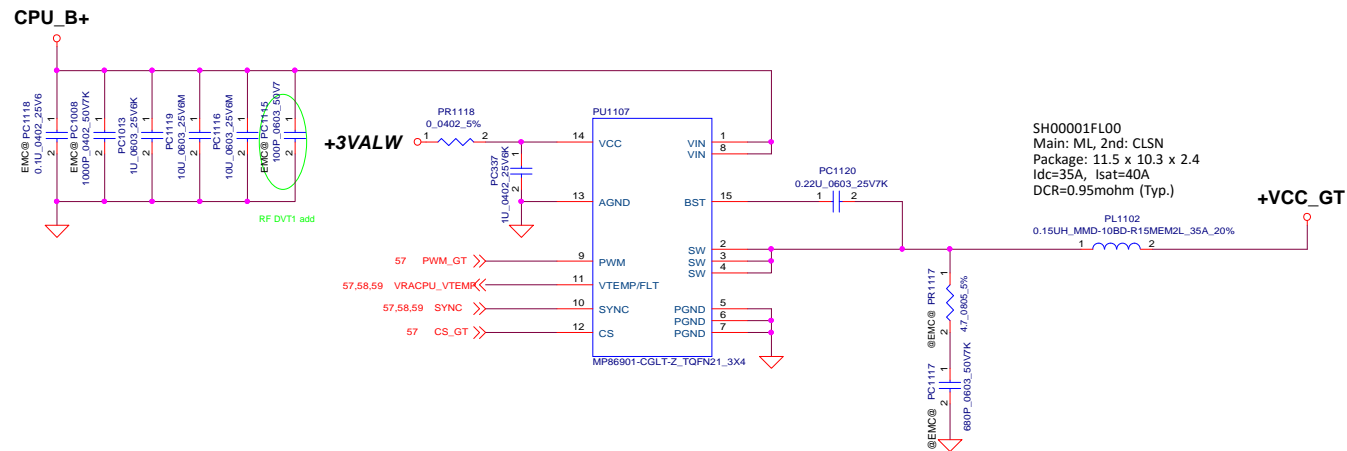


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				Size	Document Number	Revision
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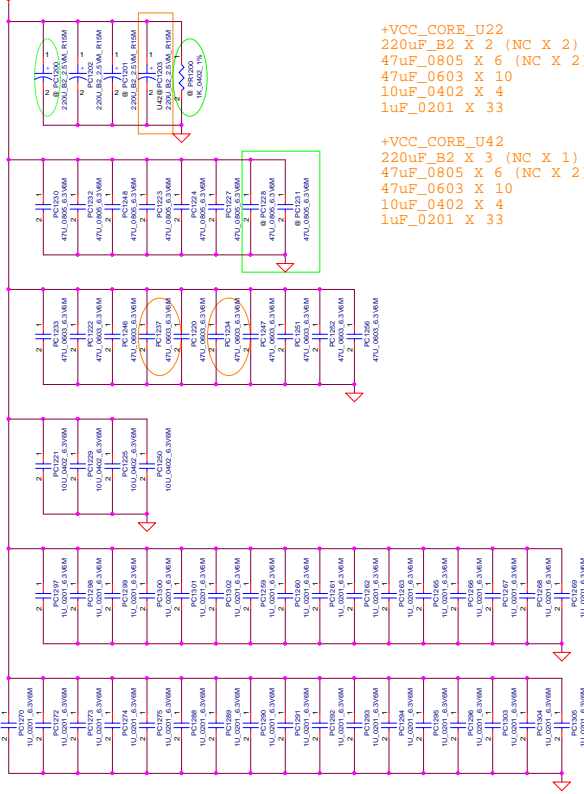
VCC\_GT/SA Dr. MOS (36.2), Support component(36.3)



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VCC\_CORE output cap[36.4], VCC\_GT output cap[36.5], VCC\_SA output cap[36.6], VCCIA\_GT output cap[36.7]

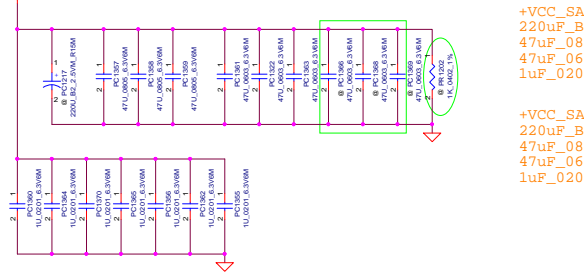
+VCC\_CORE



+VCC\_CORE\_U22  
220uF\_B2 X 2 (NC X 2)  
47uF\_0805 X 6 (NC X 2)  
47uF\_0603 X 10  
10uF\_0402 X 4  
1uF\_0201 X 33

+VCC\_CORE\_U42  
220uF\_B2 X 3 (NC X 1)  
47uF\_0805 X 6 (NC X 2)  
47uF\_0603 X 10  
10uF\_0402 X 4  
1uF\_0201 X 33

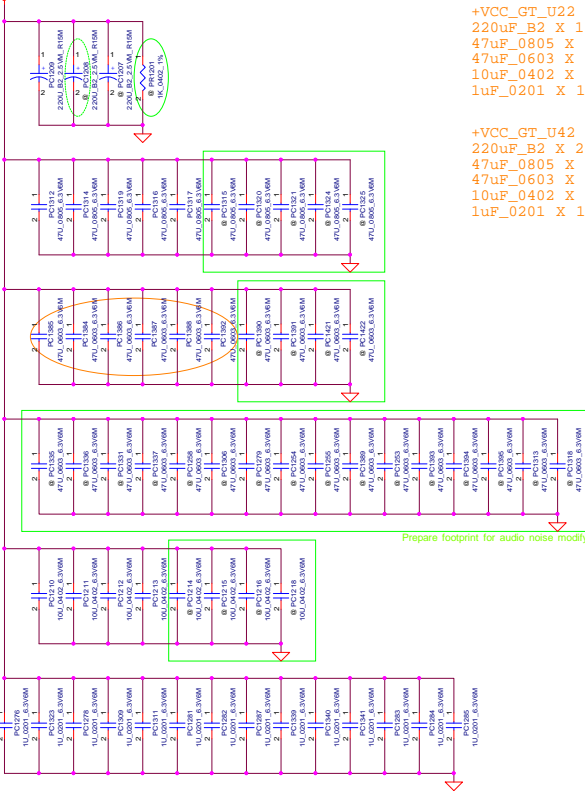
+VCC\_SA



+VCC\_SA\_U22  
220uF\_B2 X 0 (NC X 1)  
47uF\_0805 X 3  
47uF\_0603 X 3 (NC X 3)  
1uF\_0201 X 7

+VCC\_SA\_U42  
220uF\_B2 X 0 (NC X 1)  
47uF\_0805 X 3  
47uF\_0603 X 3 (NC X 3)  
1uF\_0201 X 7

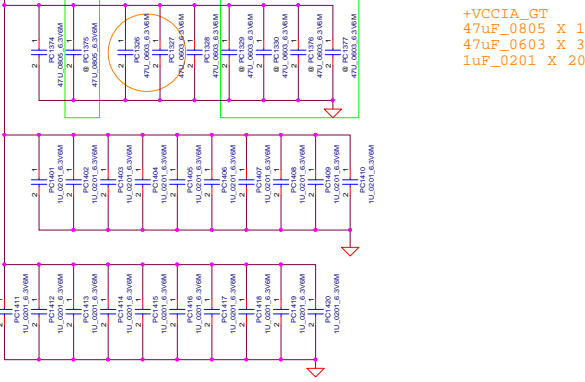
+VCC\_GT



+VCC\_GT\_U22  
220uF\_B2 X 1 (NC X 2)  
47uF\_0805 X 5 (NC X 5)  
47uF\_0603 X 6 (NC X 20)  
10uF\_0402 X 4 (NC X 4)  
1uF\_0201 X 14

+VCC\_GT\_U42  
220uF\_B2 X 2 (NC X 1)  
47uF\_0805 X 5 (NC X 5)  
47uF\_0603 X 6 (NC X 20)  
10uF\_0402 X 4 (NC X 4)  
1uF\_0201 X 14

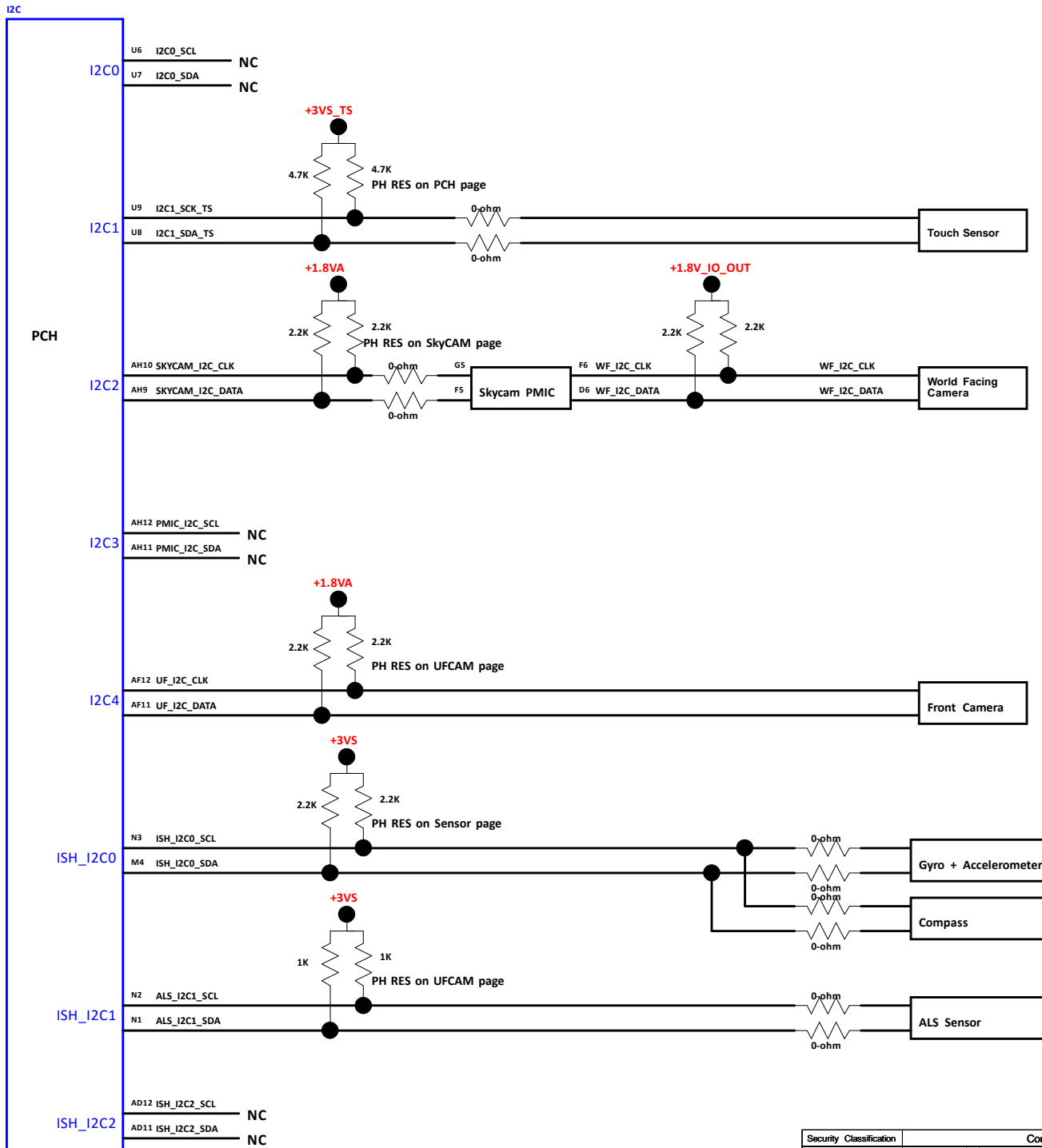
+VCCIA\_GT

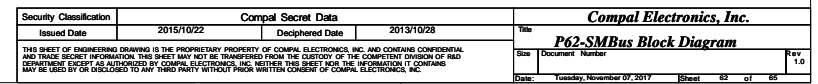


+VCCIA\_GT  
47uF\_0805 X 1 (NC X 1)  
47uF\_0603 X 3 (NC X 4)  
1uF\_0201 X 20

Prepare footprint for audio noise modify







# Discrete Power On Sequence

[AC in]

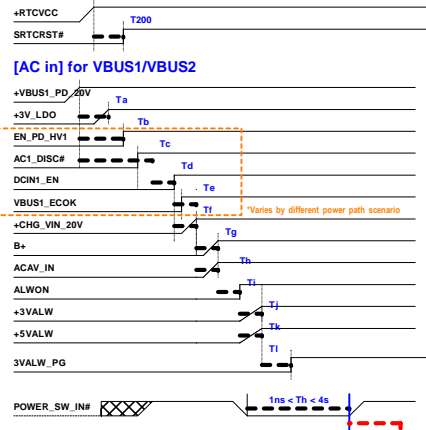
[Battery only, AC absent]

ITEM	Measure Point	Time
Ta	+VBUS_PD_20V	To
Tb	3V_LDO	To
Tc	EN_PD_HV1	To
Td	EN_PD_HV1	To
Te	AC1_DISC#	To
Tf	DCINT_EN	To
Tg	VBUS1_ECOK	To
Th	+CHG_VIN_20V	To
Ti	ACAV_IN	To
Tj	ALWON	To
Tk	+3VALW	To
Tl	+5VALW	To

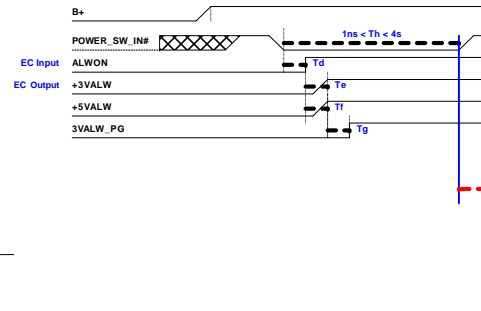
ITEM	Measure Point	Time
Ta	+VBUS_PD_20V	To
Tb	3V_LDO	To
Tc	EN_PD_HV1	To
Td	EN_PD_HV1	To
Te	AC1_DISC#	To
Tf	DCINT_EN	To
Tg	VBUS1_ECOK	To
Th	+CHG_VIN_20V	To
Ti	ACAV_IN	To
Tj	ALWON	To
Tk	+3VALW	To
Tl	+5VALW	To

ITEM	Measure Point	Time
T1	DSW_ON	To
T2	+3VALW_DSW	To
T3	+3VALW_DSW	To
T4	PCH_DPWRK	To
T5	SIO_SLP_SUS#	To
T6	PCH_PWR_EN	To
T7	PCH_PWR_EN	To
T8	PCH_PWR_EN	To
T9	PCH_PWR_EN	To
T10	PCH_PWR_EN	To
T11	PCH_PWR_EN	To
T12	PCH_PWR_EN	To
T13	PCH_PWR_EN	To
T14	PCH_PWR_EN	To
T15	PCH_PWR_EN	To
T16	PCH_PWR_EN	To
T17	PCH_PWR_EN	To
T18	PCH_PWR_EN	To
T19	PCH_PWR_EN	To
T20	PCH_PWR_EN	To
T21	PCH_PWR_EN	To
T22	PCH_PWR_EN	To
T23	PCH_PWR_EN	To
T24	PCH_PWR_EN	To
T25	PCH_PWR_EN	To
T26	PCH_PWR_EN	To
T27	PCH_PWR_EN	To
T28	PCH_PWR_EN	To
T29	PCH_PWR_EN	To
T30	PCH_PWR_EN	To
T31	PCH_PWR_EN	To
T32	PCH_PWR_EN	To
T33	PCH_PWR_EN	To
T34	PCH_PWR_EN	To
T35	PCH_PWR_EN	To
T36	PCH_PWR_EN	To
T37	PCH_PWR_EN	To
T38	PCH_PWR_EN	To
T39	PCH_PWR_EN	To
T40	PCH_PWR_EN	To
T41	PCH_PWR_EN	To
T42	PCH_PWR_EN	To

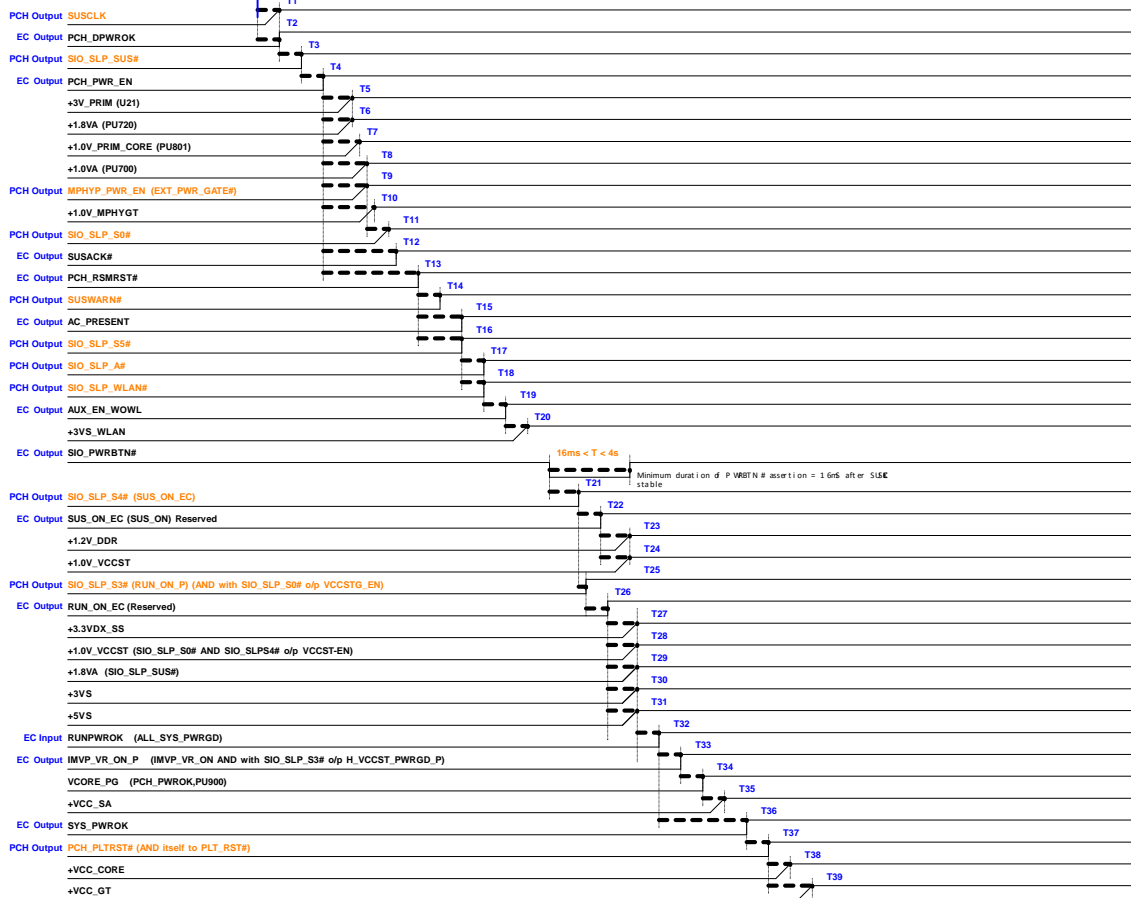
update

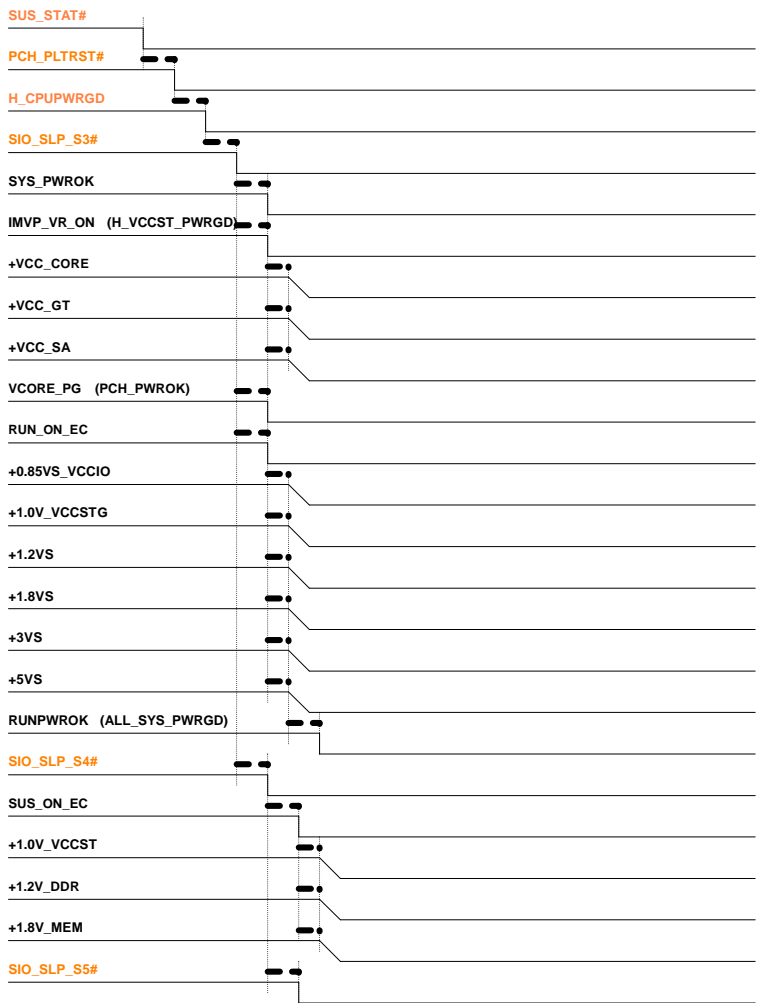


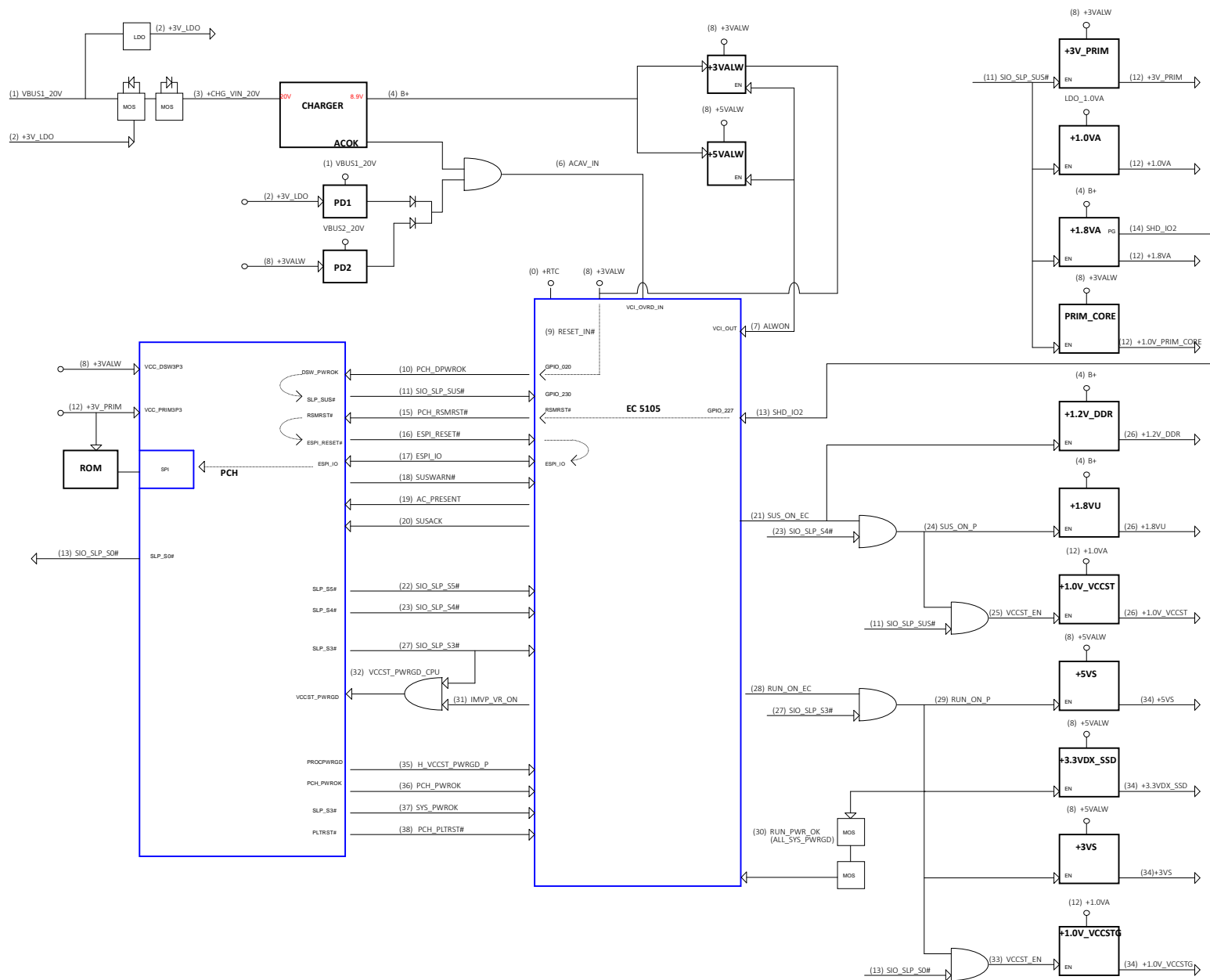
[Battery only, AC absent]



EC pay attention timing







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